Part I: Mixed-Signal Performance of Various High-Voltage Drain-Extended MOS Devices

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***Abstract*—In this paper, the optimization issues of various drain-extended devices are discussed for input/output applications. The mixed-signal performance, impact of process variations, and gate oxide reliability of these devices are compared. Lightly doped drain MOS (LDDMOS) was found to have a moderate performance advantage as compared to shallow trench isolation (STI) and non-STI drain-extended MOS (DeMOS) devices. Non-STI DeMOS devices have improved circuit performance but suffer from the worst gate oxide reliability. Incorporating an STI region underneath the gate–drain overlap improves the gate oxide reliability, although it degrades the mixed-signal characteristics of the device. The single-halo nature of DeMOS devices has been shown to be effective in suppressing the short-channel effects.**

***Index Terms*—Drain-extended MOS (DeMOS), hot carrier, input/output, lightly doped drain MOS (LDDMOS), mixed signal, reduced surface field (RESURF), reliability.**

I. Introduction

NOWADAYS, electronic systems often have multiple semiconductor chips fabricated in different CMOS technologies handling different functionalities like voltage regulation, signal conditioning, data conversion, and digital processing. Many integrated circuits like system-on-chips (SOCs) consist of multiple embedded CMOS technologies. On the other hand, with the continued scaling of devices in advanced digital CMOS technologies, the power supply voltage is also getting scaled to reduce the power consumption and to meet the gate oxide reliability. Therefore, interfacing the semiconductor chips or subsystems on the chip, having different levels of supply voltage, and satisfying the speed and noise requirements are becoming crucial from the overall performance point of view. For example, a digital processing chip working with a supply voltage of 2 V may interact with a peripheral chip with a supply voltage of 12 V. The I/O circuit design should be allowed to span the entire design space that the logic design enjoys. However, constraints like undesired leakage current paths between chips [1], [2], electrical overstress across the gate oxide [3], and hot carrier degradation [4] in I/O design take away the flexibility.

One of the bottlenecks for introducing CMOS I/O circuits is their susceptibility to electrostatic discharge (ESD). It is due to both the gate oxide breakdown and junction-degradation-related problems, caused by the decreased oxide thickness and increasing doping levels in scaled technologies [5]. The ESD problems are further aggravated by the tight design window for high-performance I/O circuits, not allowing large ESD devices to be used as protection elements [6]. This ends up reducing the number of options available to an I/O designer [7]. ESD reliability imposes the following constraints over I/O design [7]:

1) granularity in width and fixed length, which are imposed by some of the ESD rules, causing a tradeoff between the speed, area, and ESD performance of the I/O circuit;
2) ESD diode termination, which affects the I/O signal integrity because of large overshoots and undershoots of I/O voltage.

Therefore, the overall I/O performance depends on how the I/O devices are designed and optimized while considering their susceptibility to ESD protection.

Previously, mixed-signal SoC products were designed using bipolar-CMOS-DMOS (BCD) technologies [8], [9]. The trend toward lowering the system cost has favored the use of a low-cost CMOS process. It was shown that a high-voltage (HV) CMOS process can be accomplished without any additional process complexity of buried layers as in the BCD process [10]. Scaling the HV CMOS process down to the 0.13-μm node has recently been reported [11]. The published work also reports replacing the BCD process with a CMOS process in some applications that were previously dominated by the BCD technology.

HV or I/O devices are used in various applications such as broadband communication, mobile chips, smart power ICs, nonvolatile memories, microelectromechanical systems (MEMSs), etc. For high-speed data transfer on a twisted-pair copper connection, a subscriber line interface circuit integrated in CMOS technology is required [12]–[14]. Power management modules such as the high-efficiency switch-mode dc–dc converter are critical building blocks for state-of-the-art portable applications. They are used to accurately transform a battery supply into various regulated voltages, as required by their loads [15], [16]. Charge pump circuits are used to generate dc voltages higher than the nominal power supply [17], which are used in nonvolatile flash memories [18] and MEMS [19] applications. Charge pump circuits are also used in some low-voltage

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analog designs to improve the circuit performance [20]. Some other applications are low-voltage-to-HV level shifters [21] and RF power amplifiers [22]. In Part I of this paper, three types of HV I/O transistors in 130-nm CMOS technology are realized, and their performance is compared for analog/RF applications.

Part I of this paper is organized as follows. Section II will review various HV devices in CMOS technology. Section III will discuss the device realization and simulation setup, whereas Section IV will describe the intrinsic behavior and impact of process variations/misalignments over the intrinsic performance of realized devices. The analog/RF performance of the various I/O devices is compared in Section V, followed by a discussion and summary of important findings in Section VI.

II. HV Devices Compatible to CMOS Technology

Conventional MOS transistors are generally not useful for HV or I/O applications. They are designed to process information (data) by using minimum energy and the least area. The maximum drain voltage is limited by the gate oxide breakdown, avalanche breakdown, and punchthrough. This forces a change in device geometry for devices that handle HV or I/O applications [23]. Various ways of achieving HV devices in CMOS technologies are listed as follows.

1) *Lightly doped drain MOS (LDDMOS)*: By incorporating a lightly doped $(\mathrm{n}^-/\mathrm{p}^-)$ drain (LDD) region between the drain $(\mathrm{n}^+/\mathrm{p}^+)$ and the gate, as shown in Fig. 1(a), a high-drain-voltage operation can be achieved without exceeding the silicon critical electric field. The positive charge in the depleted LDD region (NMOS) is balanced by a negative charge in the p-layer underneath the LDD region. This makes the electric field nearly uniform in the lateral direction, which helps in increasing the maximum drain bias (V_{DS}) by simply increasing the length of the LDD region [24], [25]. This action is called reduced surface field (RESURF) [26], [27]. The drawback of this approach is increased resistance in the ON-state and the requirement of an additional mask [23]. It is worth mentioning that the LDD or RESURF implant and the silicide-blocking mask exist in sub-100-nm-node CMOS technologies. Increasing the LDD length linearly improves (increases) the junction breakdown voltage but leads to a degraded ON resistance (R_{ON}) and vice versa. This approach maintains a similar $R_{\mathrm{ON}}.V_{\mathrm{BD}}$ tradeoff. It should be noted down that the LDD region implant is different (in terms of the doping profile and the junction depth) from the source/drain (S/D) extension implant in a standard (sub-100-nm-node) CMOS process.
2) *Drain-extended MOS (DeMOS)*: Since advanced processes have both n-well and p-well implants, the RESURF action can be achieved by using deep n-well (NMOS) underneath the drain (n^+) region, as shown in Fig. 1(b). Gate overlap is used to suppress the junction field in the ON-state [23]. The disadvantage of DeMOS is the change in gate-to-drain field profile, but it saves a mask and an implant step, which was previously required for the RESURF implant. In this paper, this device is named as a non-shallow-trench-isolation (non-STI) DeMOS device. The gate overlap length (from the well junction to the drain edge) directly affects the breakdown voltage. Increasing the gate overlap length significantly improves the junction breakdown voltage, whereas it linearly degrades the ON resistance, eventually leading to an improved $R_{\mathrm{ON}}.V_{\mathrm{BD}}$ tradeoff. At the same time, increasing the overlap length causes an unwanted area overhead and a gate-to-drain capacitance.
3) *Shallow trench isolation (STI) DeMOS*: A high gate oxide field in DeMOS devices near the gate-to-n-well (NMOS) overlap region requires a thick oxide underneath the gate–drain overlap. This is achieved by the local-oxidation-of-silicon (LOCOS) technology, although it decreases the device density. Furthermore, hot-carrier trapping in these devices leads to an undesirable shift in electrical characteristics [28], [29]. In more recent technologies, STI has been used to create a thick-oxide

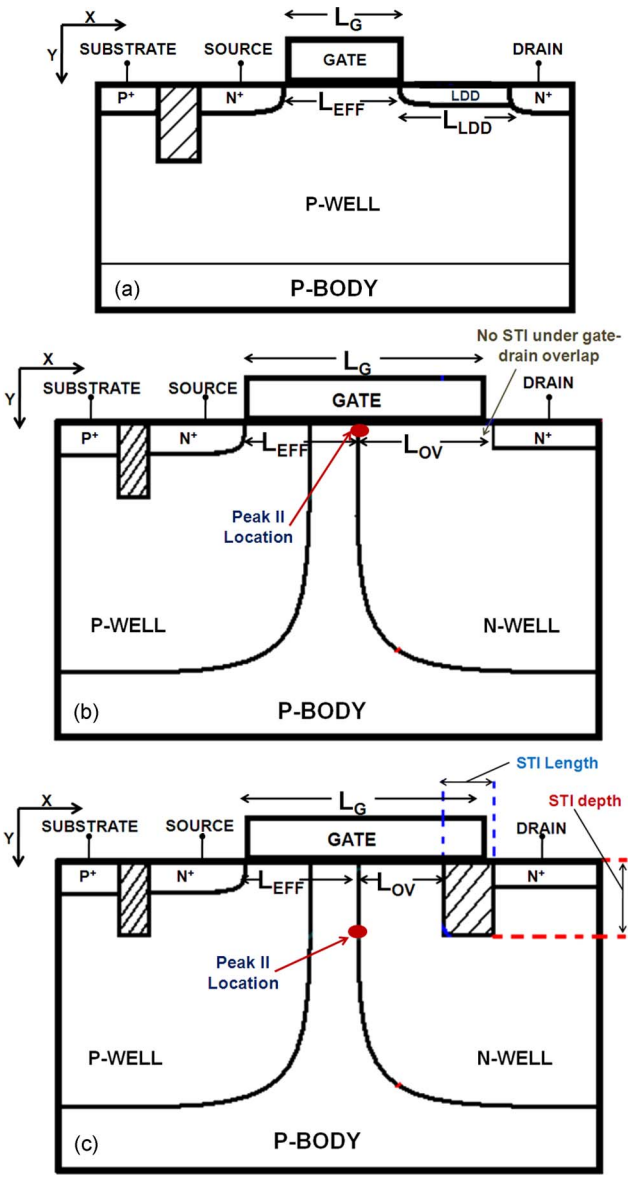

Fig. 1. Schematics of I/O devices. (a) LDDMOS. (b) Non-STI DeMOS. (c) STI DeMOS.

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TABLE I
DIMENSIONAL SPECIFICATIONS OF OPTIMIZED DEVICES

Devices	L_G (nm)	L_{EFF} (nm)	L_{OV}/L_{LDD} (nm)	STI Length (nm)
STI DeMOS	900	390	310	200
NonSTI DeMOS	900	420	480	-
LDDMOS	250	250	700	-

region, as shown in Fig. 1(c) [30], [31]. This helps in increasing the logic density by eliminating the LOCOS bird's beak, but it has a negative effect on I/O devices because of the abrupt transition introduced to the ON-state current flow [23]. It is worth to mention here that, at present, most of the HV CMOS technologies use the LDDMOS devices. The overlap length (from the well junction to the STI edge) significantly affects the ON resistance and the junction breakdown voltage. Increasing the overlap length (by keeping other dimensional parameters unchanged) up to 200 nm improves the ON resistance and reduces the breakdown voltage, whereas it shows no change after 200 nm (this length depends on the n-well profile and, eventually, on the technology node). A change in overlap length does not affect the electric field in the oxide near the drain electrode because of the STI underneath drain-to-gate edge.

Furthermore, it is worth mentioning here that the junction breakdown voltage also depends on the p-well, the n-well/LDD profile, and the spacing between p-well and n-well/LDD regions.

In Part II, we have proposed a modified HV device structure and shown its performance improvement over STI DeMOS and DeMOS (non-STI DeMOS) in terms of analog/RF behavior and hot-carrier reliability. All 2-D simulations have been carried out using the well-calibrated Sentaurus technology computer-aided design (TCAD) tool. The Sprocess process simulator was used for simulating device structures, and the Sdevice tool was used for device simulations [32], [33].

III. DEVICE REALIZATION AND SIMULATION SETUP

The devices used in this paper are realized using a well-calibrated process simulation deck. The same process flow is used for STI DeMOS and non-STI DeMOS transistors. This process is the same as the process flow of a conventional CMOS transistor, except for the n^+ drain, which is formed in the n-well region, and the n^+ source, which is formed in the p-well region. No V_T or punchthrough implant is used, and the threshold voltage of the device is adjusted by the p-well underneath the gate. Non-STI DeMOS does not have any STI in the n-well region underneath the gate–drain overlap. In these devices, the p-well underneath the source and gate acts like a single halo [34], which improves the subthreshold behavior.

The process flow for LDDMOS is the same as that for conventional CMOS, except for a large LDD region between the drain and the gate, which is used to increase the maximum drain voltage. It is required to protect the LDD region from n^+ S/D implant and silicidation (called silicide-blocking mask). The deep n-well and p-well have a retrograde profile, which is used to improve the breakdown characteristics of the device

TABLE II
ELECTRICAL SPECIFICATIONS OF OPTIMIZED DEVICES

Devices	I_{ON}	I_{OFF}	V_T	V_{BD}
STI DeMOS	590 μA/μm	1nA/μm	0.3V	23V
NonSTI DeMOS	590 μA/μm	1nA/μm	0.3V	23V
LDDMOS	590 μA/μm	1nA/μm	0.3V	13V

[35]. Implant parameters such as dose, energy, and tilt angle are calibrated to match the doping profiles extracted from secondary-ion mass-spectrometry (SIMS) measurement (SIMS plot not shown here). The gate oxide thickness (2.2 nm), spacer thickness, polysilicon height, STI depth (350 nm), etc., are kept as per the technology specification at 130-nm node. The n-well-to-p-well spacing, mask gate length, effective gate length, STI length, and gate overlap (listed in Table I) were optimized to achieve maximum $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ and breakdown voltage. The achieved I_{ON}, I_{OFF}, V_T, and V_{BD} are given in Table II.

All three realized devices are optimized for maximum breakdown voltage by keeping the same I_{ON}, I_{OFF}, and V_T. The effective channel length (L_{EFF}), LDD length (L_{LDD}) or n-well-to-gate overlap (L_{OV}), and n-well-to-p-well spacing of the devices are calibrated to achieve matched I_D–V_G characteristics. These devices are used to compare the breakdown, analog/RF performance, and scaling trends in this paper. A well-calibrated drift diffusion device simulation deck was used in this paper [33]. To study the breakdown characteristics of the device, a well-calibrated "New University of Bologna" (UniBo2) impact ionization model is used [36]. Carrier–carrier scattering is incorporated in the mobility model. Excess carrier recombination can take place via the Auger and Shockley–Read–Hall (SRH) recombination models. To incorporate this effect, the SRH and Auger recombination models are used. To take surface quantization effects into account, Van Dort's model is used for device simulation. Fig. 2(a) shows an excellent match between the experimental and simulated I–V characteristics of an NMOS device realized at the same technology node.

IV. INTRINSIC PERFORMANCE OF THE DEVICES

A. DC Characteristics

Fig. 2(b) shows the I_D–V_G plot for all the three realized devices under an equal V_{DS} voltage of 8 V. It is clear from the figure that all three devices have matched I_D–V_G characteristics. An I_{ON} value equal to 590 $\mu\mathrm{A}/\mu\mathrm{m}$, an I_{OFF} value equal to 1 $\mathrm{nA}/\mu\mathrm{m}$, and a V_T of 0.3 V are achieved.

Fig. 2(c) shows the I_D–V_D characteristics of all three devices at different gate voltages. The saturation characteristics of these devices are quite different because of their nonidentical drift regions, which leads to different drain resistance values. Non-STI DeMOS shows the best saturation characteristics and the lowest ON resistance (R_{ON}), whereas STI DeMOS shows the

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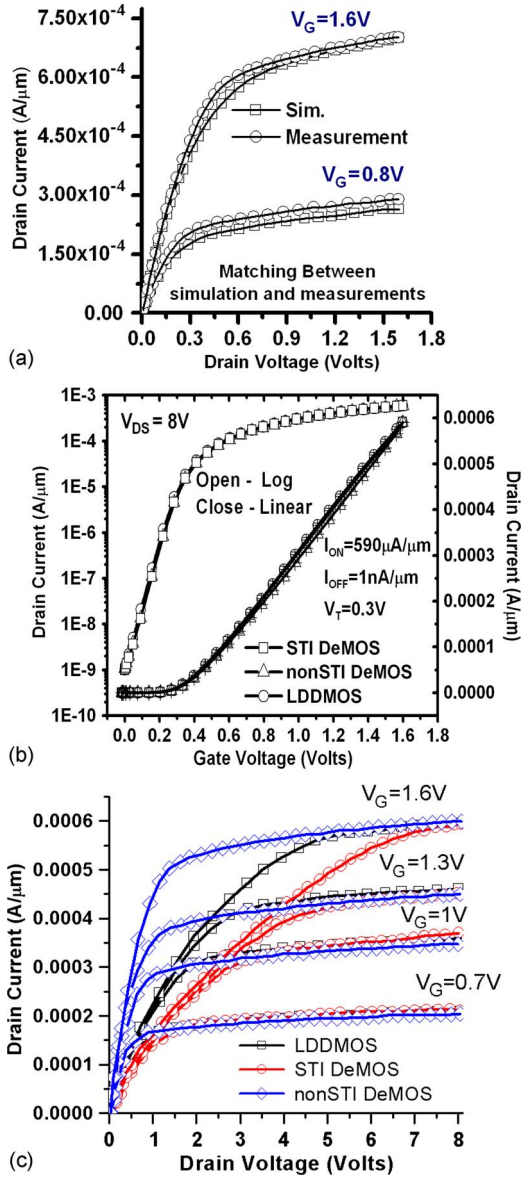

Fig. 2. (a) Matching between simulated and experimental characteristics of the reference device. (b) Device characteristics: I_D–V_G. All three devices have matched I_D–V_G characteristics. (c) Simulated I_D–V_D characteristics.

worst saturation characteristics and the highest $R_{\rm ON}$ at maximum gate bias. LDDMOS shows moderate performance.

Fig. 3 shows the breakdown characteristics of all three devices. The I_D–V_D plot is simulated with the impact ionization model turned on at $V_{\rm GS} = 0$ V. The breakdown voltage is taken as the drain voltage at which the drain current rises to ten times the nominal current, i.e., 10 nA/μm. STI DeMOS and non-STI DeMOS have an equal breakdown voltage of 23 V. It should be mentioned here that, to achieve an equal $I_{\rm ON}$, the effective channel length of STI DeMOS was kept slightly lower than that of non-STI DeMOS. The difference is, however, not too high, as can be seen from the comparable breakdown voltages between these two devices. LDDMOS has a lower breakdown voltage, because of the shallow LDD region and shorter channel length as compared to DeMOS devices. Although the breakdown voltages of STI and non-STI DeMOS devices are comparable: 1) the dependence of the breakdown

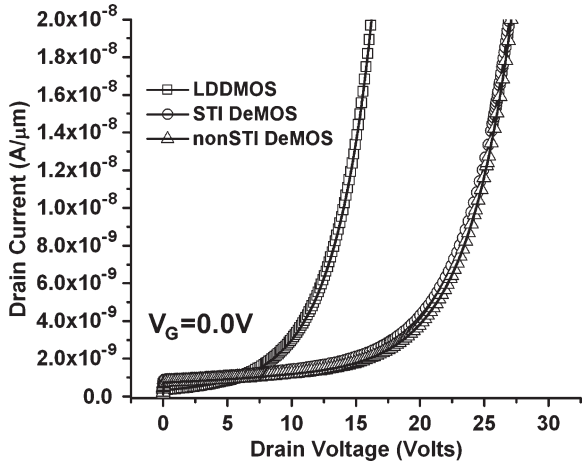

Fig. 3. Breakdown characteristics of the realized I/O devices (I_D–V_D curve at $V_G = 0$ V). The plot shows that the DeMOS has a higher $V_{\rm BD}$ compared to the LDDMOS.

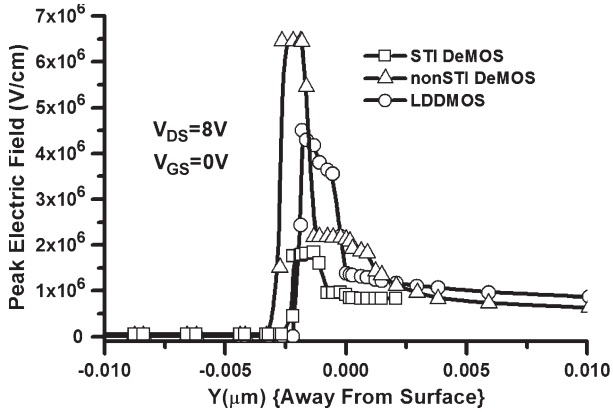

Fig. 4. Peak electric field across the gate oxide of I/O devices. Non-STI DeMOS has a higher field compared to STI DeMOS and LDDMOS.

voltage on the gate-to-n-well overlap length $(L_{\rm OV})$ is different for both devices and 2) the location of the impact ionization peak (i.e., peak electric field at the n-well–p-well junction) and its 2-D profile are different for both the STI and non-STI devices [as shown in Fig. 1(b) and (c)]. For STI DeMOS, it exists deep inside the bulk (300 nm below the surface), whereas for non-STI DeMOS, it exists closer to the surface. It is worth mentioning here that the threshold voltage of LDDMOS was optimized by using a V_T adjust implant (high doping in the channel), which leads to lower channel mobility. However, the p-well in DeMOS devices acts like a single halo, which results in a larger portion of the channel being lightly doped, giving rise to a significant improvement in channel mobility [34]. To achieve an equal $I_{\rm ON}$ for all three devices, the LDDMOS channel length is kept approximately four times lower than that of the DeMOS devices.

Fig. 4 shows the peak electric field across the gate oxide, which was extracted near the gate-to-drain edge in the overlap region. The electric field in non-STI DeMOS is three times higher than that in STI DeMOS, which shows that non-STI DeMOS is highly prone to a gate oxide breakdown. This may also lead to a gate oxide failure before junction breakdown in non-STI DeMOS. The reduced gate oxide field in STI DeMOS is because of the STI underneath the gate–drain overlap region

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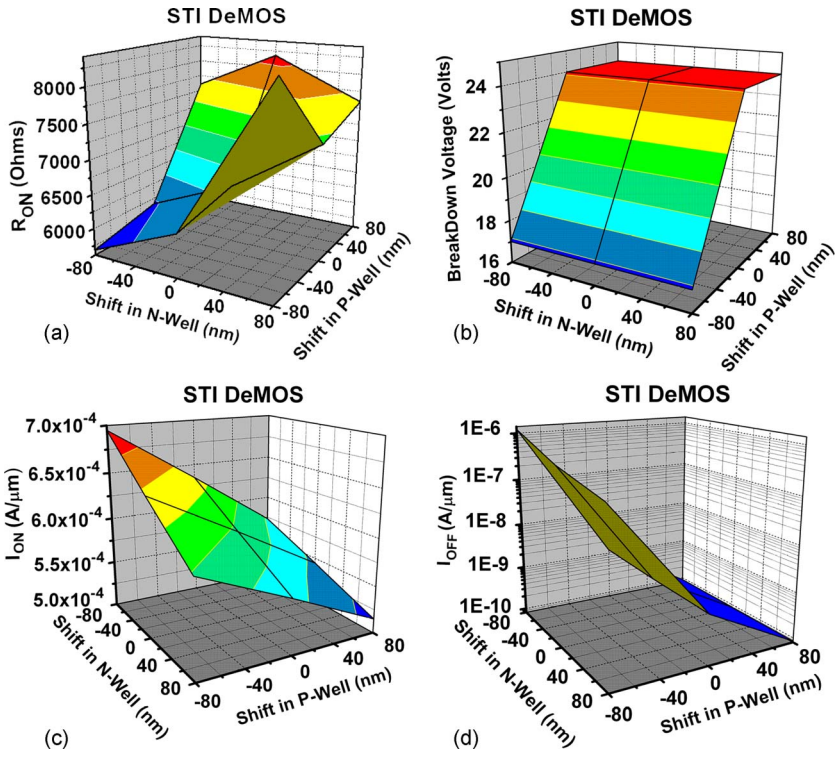

Fig. 5. Impact of process variability over intrinsic performance of STI DeMOS. (a) $R_{\rm ON}$. (b) Breakdown voltage. (c) $I_{\rm OFF}$. (d) $I_{\rm ON}$.

(spacer), which helps in relaxing the effective potential in the gate-to-n-well overlap region. Basically, the potential is more uniformly distributed in the n-well region, which was attributed to the STI underneath the gate–drain edge. This further helps in reducing the effective potential in the gate-to-n-well overlap region, which eventually leads to lower vertical electric fields. Incorporating the STI also leads to a slightly higher depletion in the gate-to-n-well overlap region, which further helps in reducing the lateral electric field near to the surface. A high gate oxide field also causes a significant increase in time-dependent dielectric breakdown and gate leakage [3], [37].

B. Impact of Process Variation and Misalignment

Variability in delay and power consumption in CMOS devices, circuits, and chips arises from process variations (or misalignment) in scaled technologies. The impact of process variations and misalignments such as variations in the STI length and n-well-to-p-well spacing on the important device parameters such as ON resistance $(R_{\rm ON})$, $I_{\rm ON}/I_{\rm OFF}$, and breakdown voltages is discussed.

Figs. 5 and 6 show the impact of a shift or misalignment in a well edge (n-well and p-well) on $R_{\rm ON}$, the breakdown voltage, $I_{\rm ON}$, and $I_{\rm OFF}$ for STI DeMOS and non-STI DeMOS. Fig. 5(a) shows the variation in $R_{\rm ON}$. $R_{\rm ON}$ is measured at a V_D equal to 0.1 V. It is clear from Fig. 5(a) that, as the n-well and p-well edges shift in the positive direction (toward the drain), the ON resistance degrades (i.e., increases) and vice versa. A positive shift in n-well increases the effective channel length, eventually leading to a higher channel resistance. A positive shift in p-well increases the threshold voltage of the device, which causes a higher channel resistance. Fig. 5(b) shows the variation in breakdown voltage with respect to the shift in the n-well and p-well edges. The breakdown voltage does not change with a positive shift in the p-well edge, whereas it reduces as it shifts toward the source because of the increase in the leakage current. The breakdown voltage does not change with variations in the n-well edge. Fig. 5(c) and (d) shows the variation in $I_{\rm ON}$ and $I_{\rm OFF}$ with respect to the shift in n-well and p-well edges. As the n-well and p-well shift towards the source side (i.e., negative direction), $I_{\rm ON}$ and $I_{\rm OFF}$ increases. A shift in n-well toward the source reduces the effective channel length, and a shift in p-well toward the source reduces the effective threshold voltage of the device, which leads to increased $I_{\rm ON}$ and $I_{\rm OFF}$. Fig. 6 shows a similar trend for non-STI DeMOS. Relatively, non-STI DeMOS shows less sensitivity to edge variations as compared to STI DeMOS because of its larger effective channel length and the difference in its impact ionization profiles.

Fig. 7 shows the impact of variation in STI length on $R_{\rm ON}$ and $I_{\rm ON}$. As the STI length increases toward the left (source side), $R_{\rm ON}$ increases, and $I_{\rm ON}$ decreases. The variation in $I_{\rm ON}$ and $R_{\rm ON}$ is less for $+/-100$ nm, but it is significant beyond $+100$ nm. Increasing the STI thickness toward the right (drain side) up to 100 nm first decreases and then increases the $R_{\rm ON}$. The increase in $R_{\rm ON}$ beyond 100 nm is because of an increase in the drain resistance. $I_{\rm ON}$ always decreases by increasing the STI thickness toward the right.

V. Analog/RF Performance Comparison of the Devices

A. Analog Performance

Fig. 8 shows the transconductance (g_m) and output resistance (R_O) of the simulated devices for a complete range of gate overdrive voltages. For a moderate gate overdrive

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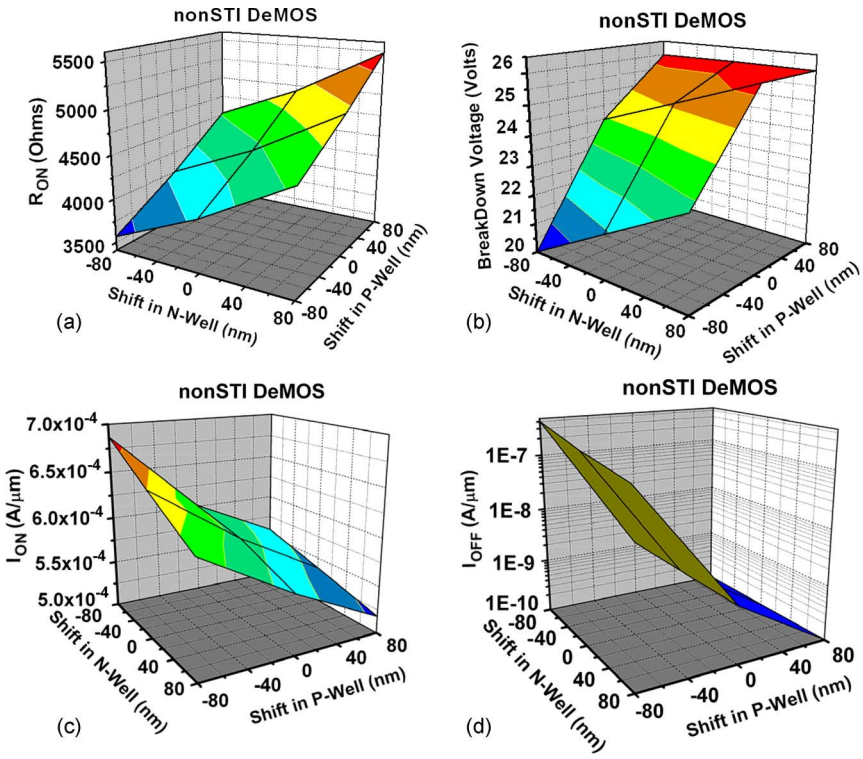

Fig. 6. Impact of process variability over intrinsic performance of non-STI DeMOS. (a) R_{ON}. (b) Breakdown voltage. (c) I_{OFF}. (d) I_{ON}.

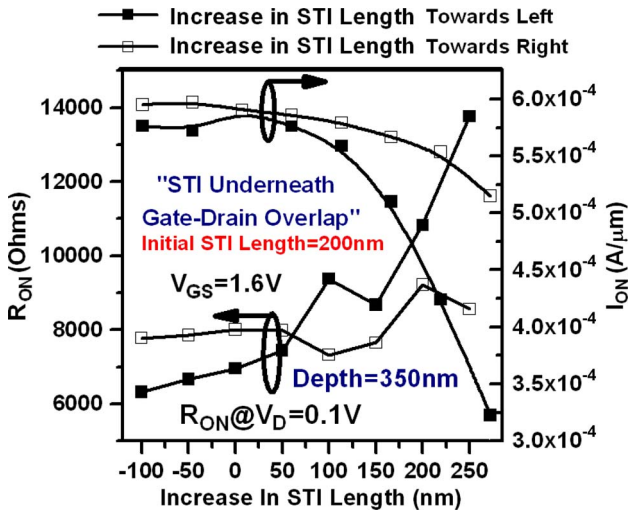

Fig. 7. Impact of variation in STI length over the turn-on behavior of a device.

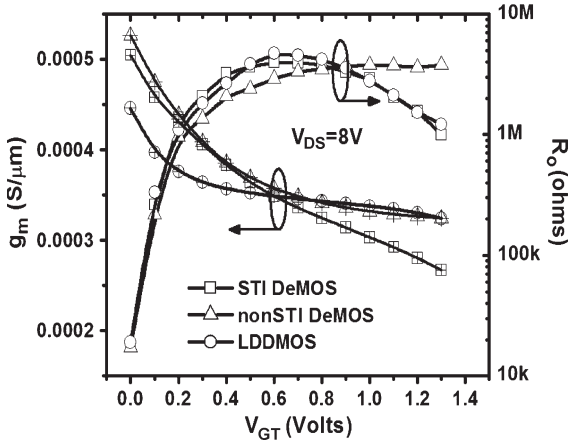

Fig. 8. Variation in transconductance (g_m) and output resistance (R_O) of all the realized devices, as a function of the gate overdrive voltage.

voltage ($V_{\mathrm{GT}} < 1$ V), the transconductance of these devices is comparable. More precisely, LDDMOS and STI DeMOS have a slightly higher transconductance, for a V_{GT} below 1 V, as compared to non-STI DeMOS. At a higher gate overdrive voltage (i.e., $V_{\mathrm{GT}} > 1$ V), non-STI DeMOS shows a significant improvement over the other two structures. Reduced drain-induced barrier lowering and channel length modulation, because of the single-halo nature of STI and non-STI DeMOS structures, contribute to the significantly higher output resistance as compared to that of the LDDMOS device at a low V_{GT}. Furthermore, the shorter channel lengths required for LDDMOS to achieve a $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ equal to that of DeMOS devices cause a degradation in the output resistance. At a higher gate overdrive voltage, STI DeMOS shows a significant degradation in output resistance because of the high drain resistance, which leads to deteriorated saturation characteristics.

Performance parameters g_m/I_D and $g_m R_O$ (intrinsic gain) of the device are also studied at a drain bias voltage of 8 V for a wide range of gate overdrive voltages, as shown in Fig. 9. Since the I_D–V_G characteristics of all the three devices are matched for performance comparisons, the performance parameter g_m/I_D for all three devices is identical and does not show any difference in performance. The intrinsic gain $(g_m R_O)$ plotted in Fig. 9 shows that the DeMOS devices consistently outperform the LDDMOS device for lower values of gate overdrive voltages. Good control of short-channel effects in DeMOS devices (because of the single-halo nature)

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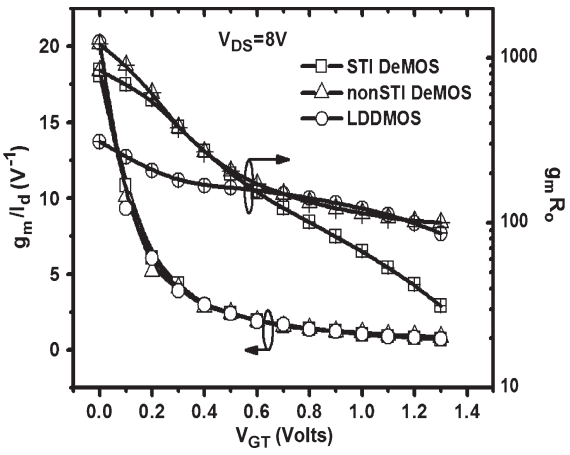

Fig. 9. Variation in performance parameters g_m/I_D and intrinsic gain $(g_m R_O)$ of all the realized devices, as a function of the gate overdrive voltage.

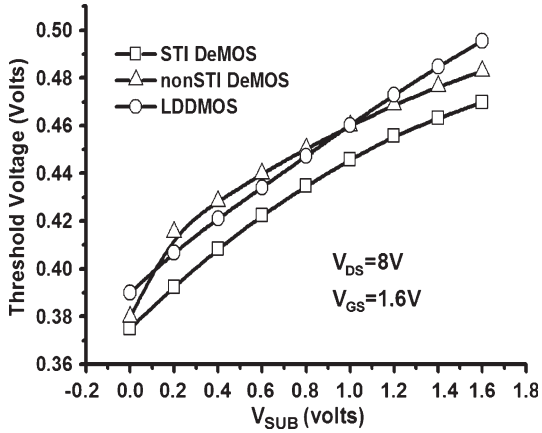

Fig. 10. Impact of the substrate bias on the threshold voltage of the various I/O devices.

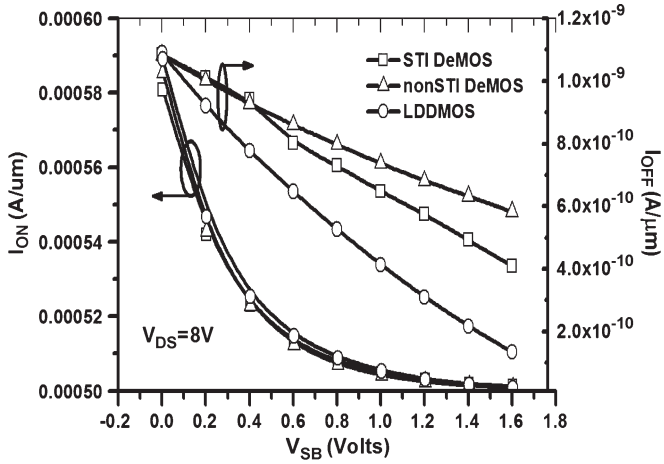

Fig. 11. Impact of substrate bias on the intrinsic performance of the realized I/O devices. The plot shows the variation in $I_{\rm ON}$ and $I_{\rm OFF}$ of all the realized I/O devices as a function of the substrate bias.

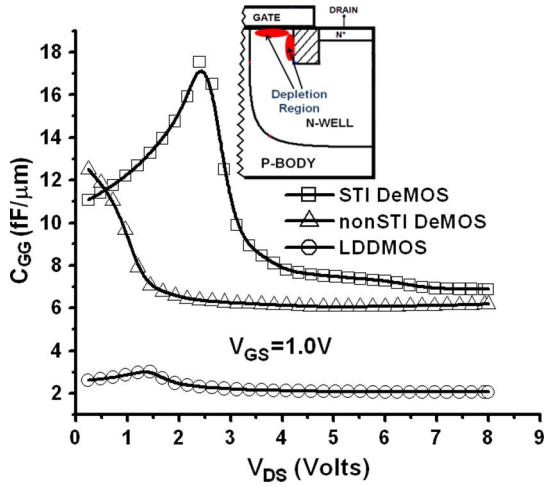

Fig. 12. Parasitic behavior of the I/O devices. The plot shows the gate-to-gate capacitance $(C_{\rm GG})$, which is the sum of gate oxide capacitance and parasitic capacitance seen by the gate terminal, as a function of the drain bias.

results in an increased $g_m R_O$ value. For a higher value of gate overdrive voltage, STI DeMOS shows a significant reduction (about 500%) in intrinsic gain because of the degradation in transconductance and output resistance, as discussed earlier.

Figs. 10 and 11 show the effect of the body bias on the device intrinsic performance. The threshold voltage, $I_{\rm ON}$, and $I_{\rm OFF}$ are plotted for a range of body bias voltages in Figs. 10 and 11. It shows that all three devices exhibit similar substrate bias sensitivity. Fig. 11 shows that the reduction in $I_{\rm OFF}$ for LDDMOS is higher as compared to that for DeMOS devices, whereas the change in $I_{\rm ON}$ with respect to the substrate bias is similar for all three devices.

Fig. 12 shows the overall gate capacitance $(C_{\rm GG})$, which includes the gate oxide capacitance $(C_{\rm OX})$, overlap, and parasitic capacitance seen by the gate terminal, as a function of the drain bias. The $C_{\rm GG}$ for LDDMOS is constant throughout the drain bias range and is significantly lower (by about three times) as compared to that for DeMOS devices. As we discussed earlier, the drawn channel length for LDDMOS is four times less as compared to that for DeMOS devices, which leads to a lower value of $C_{\rm GG}$. At a lower value of V_D, STI DeMOS shows a nonlinear behavior: $C_{\rm GG}$ first increases to a higher value, and then, it decreases. This behavior is attributed to the extra parasitic capacitance because of the depletion region around the STI and under the gate overlap. Since the depletion width of the depleted region across the STI and under the gate overlap depends on the gate and drain biases, $C_{\rm GG}$ shows a nonlinear characteristic. In Part II, we will show that this nonlinear nature gets suppressed by scaling the STI depth or, eventually, by reducing the total depletion area. For a higher drain bias, the $C_{\rm GG}$ value for STI DeMOS is 10% higher as compared to that for non-STI DeMOS.

B. Impact of Scaling on the Device Performance

Fig. 13 shows the V_T roll-off for DeMOS devices. The variation in linear V_T and saturation V_T is plotted with respect to the effective channel length of the devices. The V_T roll-off shows the same trend for both devices. There is a less than 1% variation in linear and saturation V_T, for a reduction in effective channel length from 450 to 250 nm. The effective channel length is reduced by shifting the n-well edge toward the source by keeping the rest of the process parameters identical. The negligible roll-off has been attributed to the single-halo

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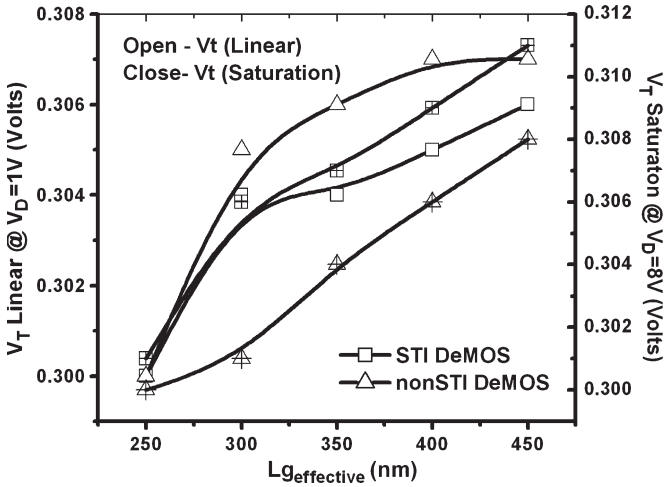

Fig. 13. Impact of scaling on the threshold voltage of DeMOS devices. The plot shows the linear and saturation threshold voltage of STI DeMOS and non-STI DeMOS as a function of the channel length.

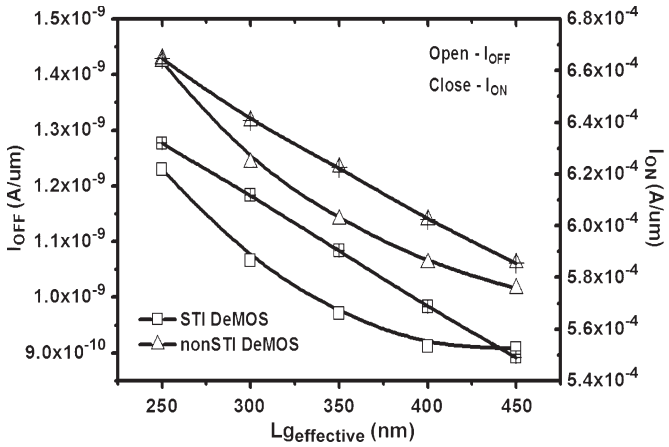

Fig. 14. Impact of scaling on the subthreshold behavior of DeMOS devices. The plot shows the $I_{\rm ON}$ and $I_{\rm OFF}$ of STI DeMOS and non-STI DeMOS as a function of the channel length.

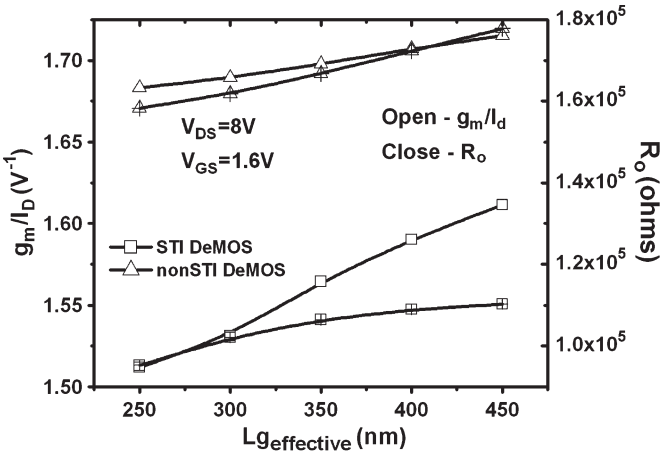

Fig. 15. Impact of scaling on the analog/RF performance of STI DeMOS and non-STI DeMOS. The plot shows the performance parameters g_m/I_D and R_O as a function of the channel length.

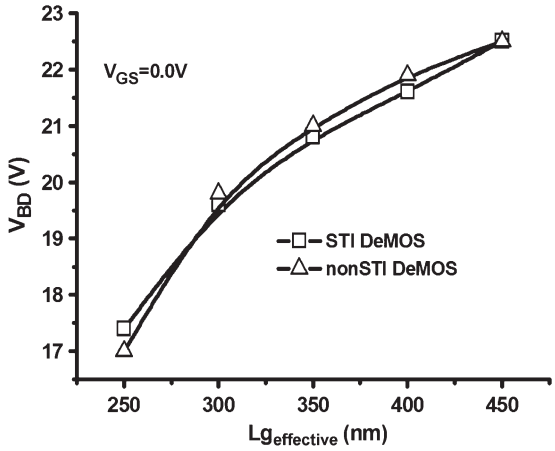

Fig. 16. Impact of scaling on the breakdown voltage of STI DeMOS and non-STI DeMOS.

nature of the DeMOS device, where the source is surrounded by a p-well that protects it from short-channel effects.

$I_{\rm ON}$ and $I_{\rm OFF}$ are plotted in Fig. 14 with respect to the effective channel length. The figure shows that the DeMOS devices are not prone to short-channel effects and that there is no significant rise in leakage current for a reduced channel length. The $I_{\rm ON}$ for non-STI DeMOS is always higher than that for STI DeMOS for any effective channel length because of the reduced drain resistance in non-STI DeMOS, as discussed earlier.

Fig. 15 shows the roll-off in performance parameters g_m/I_D and R_O with respect to the channel length. Because of the single-halo nature of the device, the degradation in performance parameters is not significant. Furthermore, it is clear from the figure that non-STI DeMOS always shows an improved performance over STI DeMOS for a range of effective channel length values. However, one needs to consider the degradation in breakdown voltage because of the reduced effective channel lengths. Fig. 16 shows that the breakdown voltage is reduced from 23 to 17 V for a reduction in effective channel length from 450 to 250 nm, which is still acceptable for I/O applications.

VI. Conclusion

In this paper, three optimized I/O devices, namely, the LDDMOS, STI DeMOS, and non-STI DeMOS devices, have systematically been compared using an extensive TCAD-based framework. LDDMOS (RESURF device), which is widely in use, shows moderate performance as compared to other two devices but exhibits a very low breakdown voltage and severe gate oxide reliability issues in scaled technology nodes. Non-STI DeMOS has a higher breakdown voltage as compared to that of LDDMOS and shows improved analog/RF performance over the other two devices but suffers from the worst gate oxide reliability. Incorporating an STI region underneath the gate–drain overlap suppresses the peak gate oxide electric field, but it significantly increases the drain resistance, which eventually degrades the saturation and turn-on characteristics of the device. This causes the degraded analog performance of STI DeMOS as compared to that of the other two devices. The single-halo nature of DeMOS devices improves the scalability of these devices and also suppresses the short-channel effects. Since STI DeMOS has a less effective channel length as compared to non-STI DeMOS, for the same $I_{\rm ON}$ and $I_{\rm OFF}$, it

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TABLE III
PERFORMANCE COMPARISON OF REALIZED DEVICES

FIELDS	STI DeMOS	NonSTI DeMOS	LDDMOS
Breakdown Voltage	H	H	L
Oxide Elec. Field	L	H	M
G_m	L	H	L
R_O	L	H	H
Intrinsic Gain	L	H	M
Sub. Bias Sensitivity	L	L	L
Scalability	H	H	-
Parasitic Capacitance (Normalized with gate area)	H	M	M
Parasitic Capacitance (Abs)	H	M	L

H-High
M-Moderate
L-Low

has a higher sensitivity to process variations. The performance characteristics of all these devices are summarized in Table III.

In the second part of this paper, we have shown further optimization of the STI DeMOS to achieve analog/RF performance similar to that of non-STI DeMOS without sacrificing on the gate oxide and hot-carrier injection reliability advantages of these devices.

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