# Part II: A Novel Scheme to Optimize the Mixed-Signal Performance and Hot-carrier Reliability of Drain-Extended MOS Devices

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***Abstract*—The impact of scaling the depth of the shallow trench isolation (STI) region, underneath the gate-to-drain overlap, on the STI drain-extended metal–oxide–semiconductor (DeMOS) mixed-signal performance and hot-carrier behavior is systematically investigated in this work. For the first time, we discuss a dual-STI process for input/output applications. Furthermore, the differences in the hot-carrier behavior of various drain-extended devices are studied under the ON- and OFF-states. We found that the non-STI DeMOS devices are quite prone to failure when compared with the STI DeMOS devices in both the ON- and OFF-states. We introduced a more accurate way of predicting hot-carrier degradation in these types of devices in the ON-state. We show that scaling the depth of the STI underneath the gate is the key for improving both the mixed-signal and hot-carrier reliability performances of these devices.**

***Index Terms*—Drain-extended metal–oxide–semiconductor (DeMOS), hot carrier, input/output (I/O), mixed signal, reliability, shallow trench isolation (STI).**

## I. Introduction

THE DEVICE dimensions and supply voltage of core CMOS logic have systematically been scaled down during the last few decades in order to improve the intrinsic performance of CMOS devices and suppress the hot-carrier-induced (HCI) degradation effects. However, this is not true for input/output (I/O) devices, which are used to interface the CMOS chip to peripherals operating at higher levels of supply voltage. In the early 1980s, hot-carrier degradation was a major reliability concern when device dimensions were scaled without the associated $V_{DD}$ scaling [1]. Since HCI degradation is a voltage-driven phenomena, it ceased being a dominant mechanism of degradation in the mid-1990s due to $V_{DD}$ scaling. So far, various groups have explored classical hot-carrier degradation, the results of which are summarized here.

1) HCI degradation is due to hot carriers produced by impact ionization (II) of the source current, which is maximum at $V_G \sim V_D/2$ [2]–[6].
2) Degradation is due to broken Si–H bonds at the Si–$SiO_2$ interface [7], [8] and is uncorrelated with other degradation mechanisms such as time-dependent dielectric breakdown (TDDB), which is because of the broken Si–O bonds [9]–[11] or negative bias temperature instability [12].
3) Interface damage shows a power law behavior ($\delta N_{\rm IT} = {\rm At}^n$), where time exponent $n$ has a universal value close to 0.5.
4) Interface damage anneals back after the removal of stress [12], [13].

I/O devices, which have a high operating bias voltage, are often prone to reliability issues different from those of core devices. A few groups have explored the hot-carrier reliability in I/O devices, and these results are summarized here.

1) Interface trap generation in spacer oxide becomes the dominant mechanism, which degrades the ON resistance $R_{\rm ON}$ and transit frequency $F_T$ [14]–[16].
2) OFF-state degradation because of II caused by the band-to-band tunneling (BTBT) current is more severe than the inversion-mode degradation and is an important concern as oxide thickness scales down [17], [18].
3) OFF-state degradation has a high time exponent close to 0.7 and is because of broken Si–O bonds, which cannot be annealed back. The degradation is also correlated with TDDB [17], [18].

In the first part of this paper, it was shown that there is always a tradeoff between the breakdown voltage, gate oxide reliability, and device analog/RF/mixed-signal performance. In this part, we propose a novel way for further optimization of STI DeMOS to achieve analog/RF performance that is equivalent to that of non-STI DeMOS and hot-carrier reliability similar to that of STI DeMOS. Section II will further discuss the optimization of STI DeMOS, and Section III will compare the proposed engineered device with STI and non-STI DeMOS in terms of hot-carrier reliability. Section IV will summarize the important results of this work.

## II. Optimization of STI DeMOS

Here, for the first time, we propose a dual-STI process for DeMOS devices in order to improve their analog/RF

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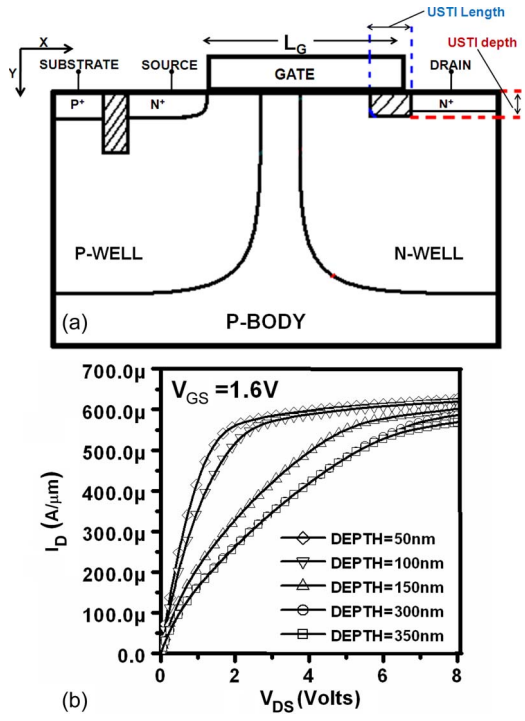


Fig. 1. (a) Standard STI DeMOS. The depth of STI, which is shown in figure, is scaled to realize USTI DeMOS. (b) $I_D$–$V_D$ characteristics of STI DeMOS with different STI depths.

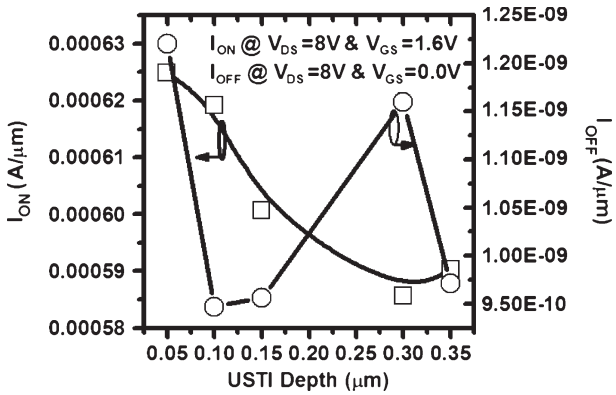


Fig. 2. Intrinsic behavior of the STI DeMOS device for different STI depths.

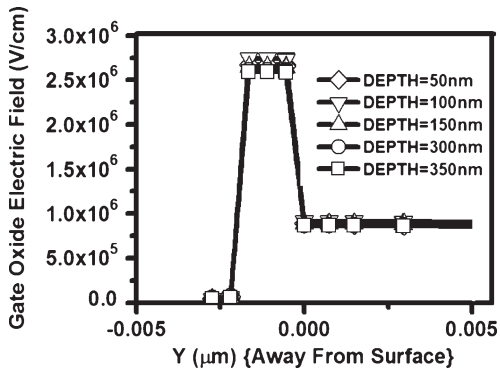


Fig. 3. Gate oxide field at $V_D = 8$ V and $V_G = 0$ V in STI DeMOS with different STI depths.

performance and long-term reliability. The gate oxide reliability, analog/RF performance, and process variations are critical aspects in the DeMOS device optimization.

### *A. USTI DeMOS*

Fig. 1(a) shows the ultrashallow trench isolation (USTI) DeMOS structure realized using the dual-shallow-trench-isolation (STI) process. The STI shown toward the left of the device is used for device isolation, whereas the USTI underneath the gate-to-drain overlap is used to attenuate the gate oxide field, which eventually gives rise to an improved long-term reliability of the device. In this section, we show the impact of scaling of the USTI depth over the analog/RF performance improvement of DeMOS devices. Due to the STI in n-well, carriers drift from the gate/n-well overlap to the drain contact through the deep n-well region (i.e., underneath STI). In this case, since the well has a retrograde profile, the depth of STI defines the average doping of the drift region. Fig. 1(b) shows the $I_D$–$V_D$ characteristics at $V_G = 1.6$ V. The figure shows an improvement in the saturation characteristics of the device as the STI depth is getting scaled from 50 to 350 nm. This is attributed to a reduced drain resistance because of the reduction in the depth of STI under the gate-to-drain overlap.

Fig. 2 shows the intrinsic behavior of the device with respect to the scaled USTI depths. $I_{\rm ON}$ shows an improvement, as the USTI depth reduces, except for the USTI depth of 300 nm, which is attributed to the retrograde nature of the well doping. There is no significant change in $I_{\rm OFF}$ with STI scaling. It is clear from the figure that peak $I_{\rm ON}/I_{\rm OFF}$ occurs at a depth of 100 nm. In addition, from Fig. 1(a), it is clear that there is only a slight difference between the characteristics of the device having USTI depths of 50 and 100 nm. For further studies, we choose a USTI depth of 100 nm. Furthermore, in order to reduce the depth variability, a USTI depth of 100 nm could be a better option, compared with a depth of 50 nm.

Fig. 3 shows the peak gate oxide field at scaled USTI depths. There is no increment in the peak gate oxide field (in the gate/n-well overlap region) with respect to reduced USTI depth. For depths ranging from 350 to 50 nm, the peak field is in the range of 2.8–2.6 MV/cm, which is comparable to a peak gate oxide field in STI DeMOS (as shown in Part I) and three to four times less than the oxide breakdown field. The relaxed gate oxide field in USTI DeMOS shown in Fig. 3 and improved intrinsic performance shown in Figs. 1(b) and 2 also give an idea about improvement in device analog/RF performance without degrading the gate oxide reliability. These topics are discussed in detail.

It is also important to discuss the breakdown characteristics of USTI DeMOS before proceeding for their analog/RF performance characteristics. The breakdown voltage of DeMOS devices is dominated by well profiles. The deep n-well underneath the drain helps in suppressing the fields, which eventually leads to a high breakdown voltage without significantly increasing the drain resistance. A high drain resistance degrades the mixed-signal performance of the device. In laterally diffused metal oxide semiconductor (LDDMOS) devices, a high breakdown voltage leads to a very high drain resistance, which degrades its mixed-signal performance. Fig. 4 shows variation in junction breakdown voltage with respect to the depth of USTI, which shows that scaling of the STI (underneath gate-to-drain overlap)

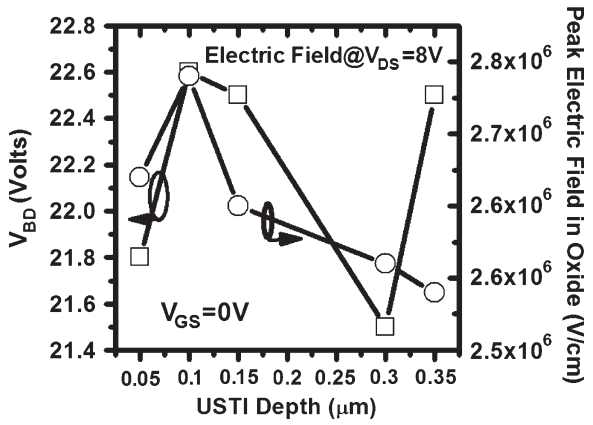


Fig. 4. Impact of USTI depth on $V_{\rm BD}$ and peak electric field in $G_{\rm OX}$. No degradation in breakdown voltage and an increase in $G_{\rm OX}$ fields are shown.

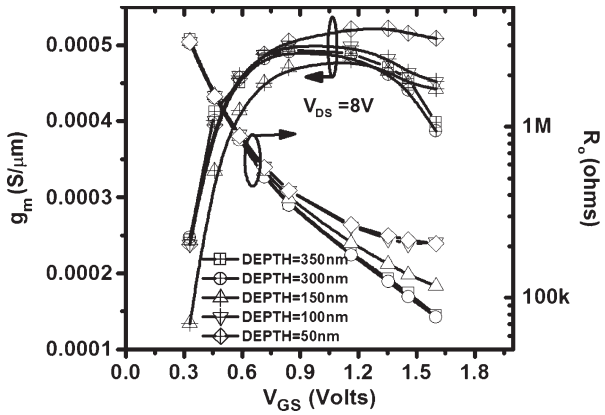


Fig. 5. $g_m$ and $R_O$ of STI DeMOS with different STI depths.

depth between 50 and 350 nm does not degrade the breakdown voltage. A variation in breakdown voltage of 5% is caused by a slight variation in the n-well/p-well junction electric field, which is attributed to the reduced resistance of the drift region (n-well) while scaling the STI depth from 350 to 50 nm. The random trend is attributed to the retrograde nature of the n-well, which was previously discussed.

### B. Analog/RF Performance Improvement

Fig. 5 shows the transconductance $g_m$ and output resistance $R_O$ of the device with respect to the gate voltage for different values of the USTI depth ranging from 50 to 350 nm at $V_{DS} =$ 8 V. The scaled USTI depth leads to a reduced effective series resistance of the drain, which eventually helps in improving the transconductance of the device. This improvement is significant for higher gate voltage. The improved saturation characteristics, as discussed earlier, helps in improving the output resistance of the device, which is again significant for a higher gate bias.

Fig. 6 shows the performance parameters $g_m/I_D$ and intrinsic gain $g_mR_O$ of the device with respect to the gate voltage for different values of USTI depth ranging from 50 to 350 nm at $V_{DS} = 8$ V. There is no significant change in $g_m/I_D$, but intrinsic gain improves for scaled USTI depths. This is attributed to the improvement in $g_m$ and $R_O$, as we discussed earlier.

The overall gate capacitance $C_{GG}$ is plotted in Fig. 7 as a function of drain bias $V_{DS}$ for USTI depths ranging from

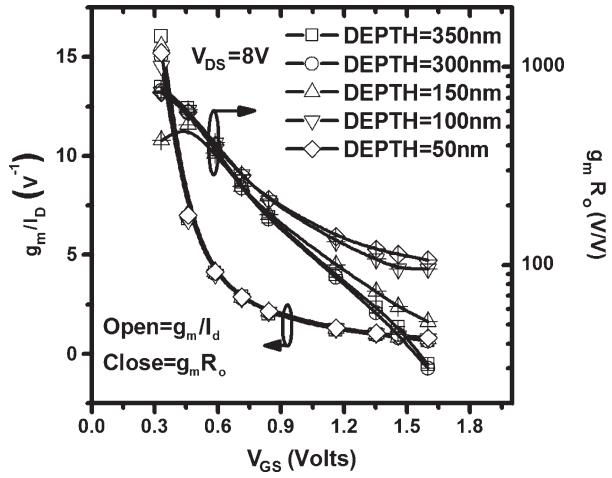


Fig. 6. $g_m/I_D$ and $g_mR_O$ of STI DeMOS with different STI depths.

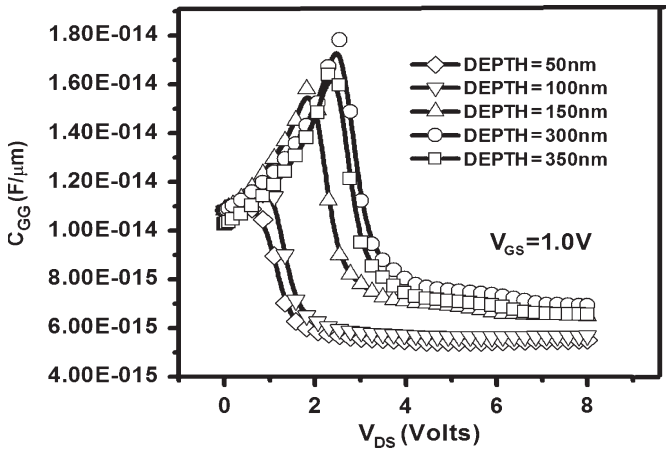


Fig. 7. $C_{\rm GG}$ as a function of drain bias for different STI depths. This shows an improvement for scaled STI depths.

50 to 350 nm at $V_{GS} = 1$ V. $C_{GG}$ is the sum of gate–oxide capacitance $C_{\rm OX}$ and parasitic capacitance seen by the gate terminal. The figure shows that scaling of the STI depth helps in reducing the overall parasitic capacitance seen by the gate terminal up to about 80% at lower drain bias $V_{DS} \sim 2$ V and about 10% at higher drain bias. This improvement is attributed to a reduced depletion capacitance, which arises because of the depleted region around STI (under gate-to-drain overlap). The reduction in depleted area is because of the lower trench area covered by the ultrashallow trench (depth $= 100$ nm), compared with STI having a depth of 350 nm. It also helps in suppressing the nonlinear behavior at low drain bias values.

### C. Impact of Process Variations and Misalignment

In this section, the impact of process variations and well edge misalignment over critical performance parameters, such as ON resistance $R_{\rm ON}$, $I_{\rm ON}$, $I_{\rm OFF}$, and breakdown voltage $V_{\rm BD}$, are discussed for USTI DeMOS having an STI (underneath gate-to-drain overlap) depth of 100 nm. Fig. 8 shows the impact of variation/misalignment of well edge (n-well and p-well) over device parameters for USTI DeMOS. Fig. 8(a) shows that, as the n-well and p-well shift in the positive direction (toward drain), $R_{\rm ON}$ increases, and vice versa. The variation is because

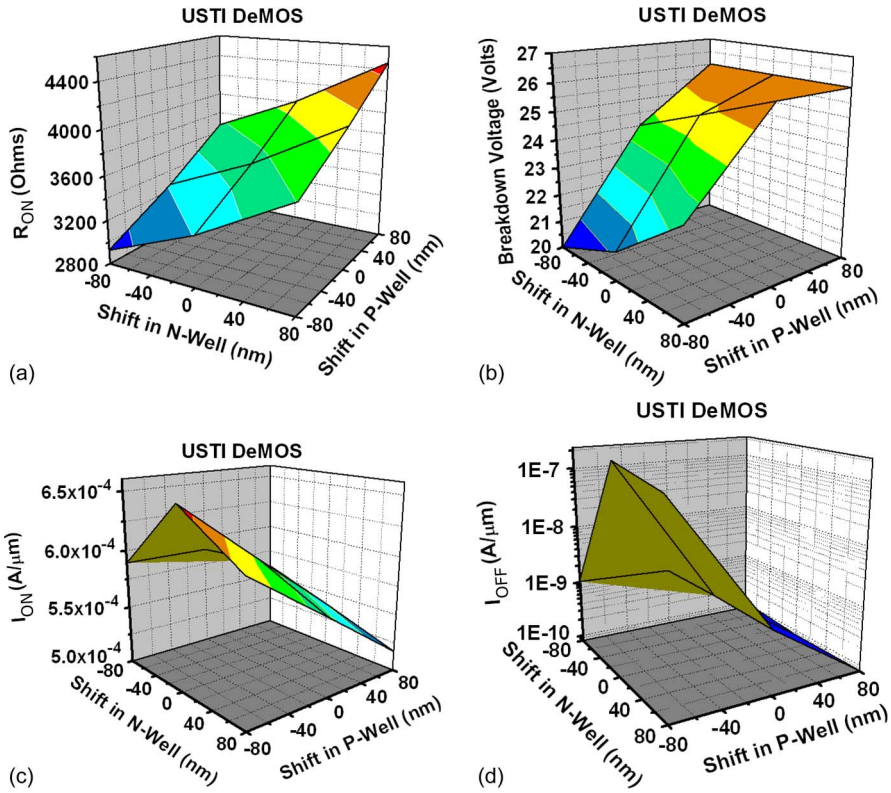


Fig. 8. Impact of variation in well spacing on the device intrinsic and turn-on behavior. (a) ON resistance at $V_D = 1$ V and $V_G = 1.6$ V. (b) Junction breakdown voltage at $V_G = 0$ V. (c) ON current at $V_D = 8$ V and $V_G = 1.6$ V. (d) OFF current at $V_D = 8$ V and $V_G = 0$ V.

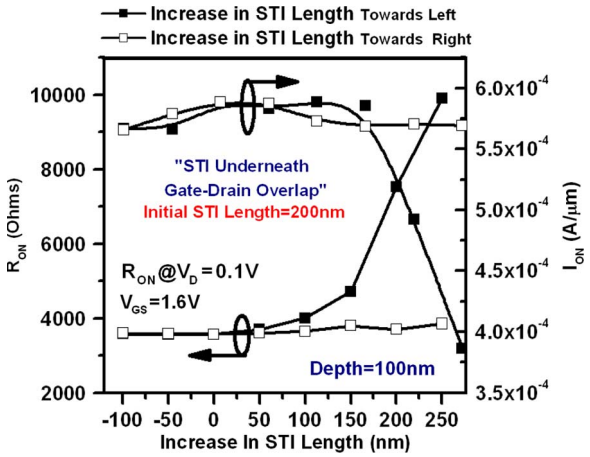


Fig. 9. Impact of variation in STI (underneath the gate overlap) length (depth = 100 nm) on the turn-on behavior.

of similar arguments as given in Part I, but the variation in $R_{\rm ON}$ is less, compared with STI DeMOS, and is similar to non-STI DeMOS. Similarly, Fig. 8(b) and (c) shows variation in $V_{\rm BD}$ and $I_{\rm ON}$, respectively, which shows a similar trend as discussed in Part I. Fig. 8(d) shows the impact of variation of well edge over leakage current $I_{\rm OFF}$. The trends are similar to STI and non-STI DeMOS, and are mostly dominated by the p-well edge. The percentage of variation in $I_{\rm OFF}$ is one order less than the variation in STI DeMOS, which shows an improved performance of USTI DeMOS over STI DeMOS in terms of process variability.

Fig. 9 shows the impact of variation in STI length on $R_{\rm ON}$ and $I_{\rm ON}$ in USTI DeMOS. As the USTI length increases toward right (i.e., toward drain), there is no change in $R_{\rm ON}$ and $I_{\rm ON}$. This behavior is different from STI DeMOS, as we discussed in Part I. Increasing the STI length toward left (i.e., toward source) significantly increases the $R_{\rm ON}$ and decreases the $I_{\rm ON}$. $R_{\rm ON}$ for USTI DeMOS is less, compared with that for STI DeMOS, and is almost equal to $R_{\rm ON}$ for non-STI DeMOS. However, all of these devices exhibit a similar turn on behavior as a function of the STI (USTI) thickness. The amount of variation in USTI DeMOS is less, compared with that in STI DeMOS, which shows a performance improvement.

## III. Hot-Carrier Reliability

In the previous sections, the performance of DeMOS devices was explored, and further optimization options for improved analog/RF performance and gate oxide reliability were discussed. In this section, another reliability issue, i.e., hot-carrier reliability of USTI DeMOS, will be compared with that of STI and non-STI DeMOS devices. The hot-carrier degradation mechanism is well known for core devices, whereas a new degradation mechanism for DeMOS devices has been introduced in [18]. In continuation, both types of degradation mechanism for DeMOS devices will be studied using full-band Monte Carlo (MC) analysis.

### A. Inversion-Mode (on-State) Degradation

For standard devices, it is well known from experimental and theoretical observations that maximum hot-carrier generation occurs at $V_G \sim V_D/2$ and strongly depends on the gate bias [1],

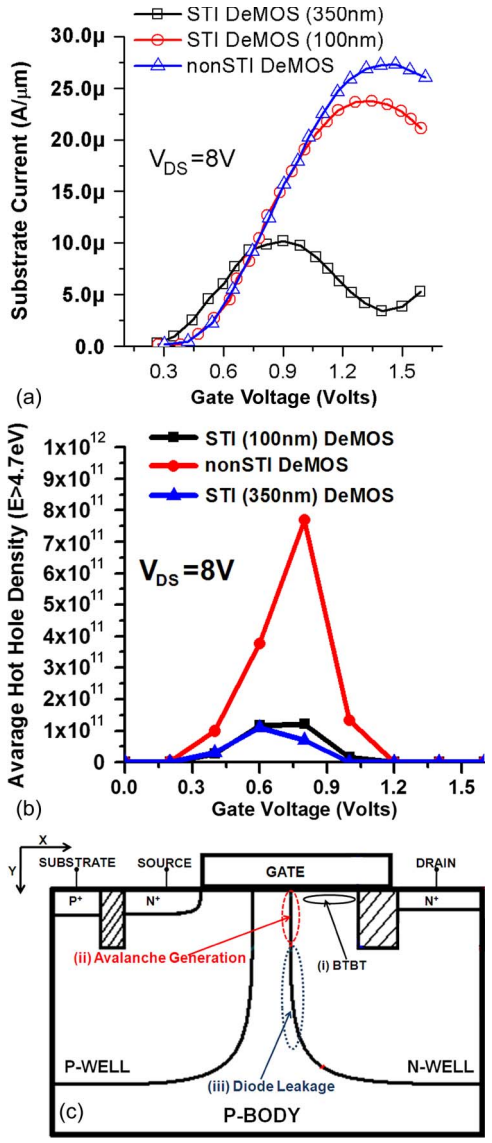


Fig. 10. (a) Substrate current ($I_{\rm SUB}$) for all DeMOS structures from drift diffusion simulation. (b) Average hot hole ($E > 4.7$ eV) density ($\rm cm^{-3}$) extracted 1 nm below the surface from MC simulations. HCI trends indicate superior reliability for scaled STI devices. (c) Differences in the location of hole generation, which explains the higher substrate current and the improved HCI reliability for shallow STI devices.

[3], [4]. For DeMOS devices, it is very important to understand and compare the hot-carrier behavior on the device ON-state. Fig. 10(a) shows the substrate current $I_{\rm SUB}$ as a function of gate bias at $V_D = 8$ V for all the three DeMOS devices. $I_{\rm SUB}$ is a good measure of hot-carrier degradation in core devices. From Fig. 10, it can be observed that 1) the peak of hot-carrier generation (or HCI degradation) occurs at a different gate bias for all DeMOS devices and that it depends on the device geometry and 2) hot-carrier degradation is less than half for STI DeMOS, compared to other devices (based on technology computer-aided design (TCAD) predictions).

Since hot holes generated from the II of the source current produce interface traps and get injected into the gate oxide to cause bulk traps or TDDB, we have plotted the average hot hole density in Fig. 10(b), which was extracted at 1 nm below the surface with respect to the gate voltage for all the three devices. From Fig. 10(b), one can observe that 1) the peak of hot-carrier generation (or eventually degradation) happens at $V_G \sim 0.8$ V ($V_D = 8$ V) for all the devices and it does not depend on geometry and 2) the hot-carrier generation for non-STI DeMOS is significantly higher (by up to a factor of 8), compared with that for USTI and STI DeMOS devices. However, USTI DeMOS has a similar hot-carrier behavior as STI DeMOS.

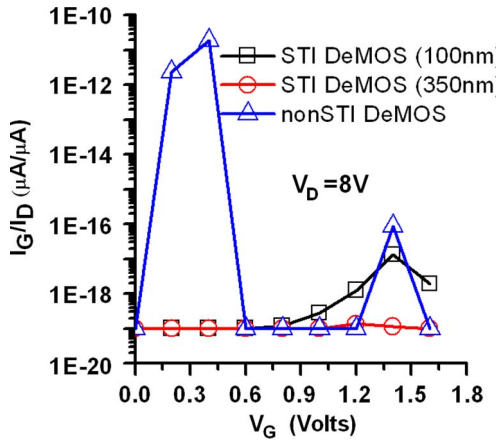


Fig. 11. $I_G/I_D$ as a function of gate bias extracted from MC simulations.

The conclusions from Fig. 10(a) and (b), which seem to be contradicting, can be interpreted in the following way: First, the substrate current consists of three components: 1) the junction leakage (from n-well to p-well); 2) the holes generated by II along the source current path; and 3) the BTBT current generated underneath the gate. The location of all these current sources is shown in Fig. 10(c). Second, the HCI degradation is only due to the hot holes (electrons) generated near the Si-$SiO_2$ interface and not the hot carriers occurring deep inside the bulk. Thus, it can be concluded that the substrate current cannot be taken as a measure of HCI degradation for DeMOS devices. It is also worth mentioning here (based on TCAD results) that the USTI DeMOS exhibits hot-carrier reliability that is very similar to that of the STI DeMOS, which is significantly higher (less hot-carrier generation near interface), compared with that of non-STI DeMOS.

Fig. 11 shows $I_G/I_D$ with respect to the gate bias extracted from full-band MC simulations for all the three devices. The non-STI DeMOS device has a significantly higher gate current, whereas the STI and USTI DeMOS have negligible current flowing through the gate at lower $V_G$. This can be attributed to very high gate oxide fields (at the gate-to-drain edge) and hot-carrier density in non-STI DeMOS devices, compared with other two structures at low $V_G$. Furthermore, increasing the gate bias causes a depletion in the gate/n-well overlap region, which increases the drain-to-gate tunnel width. This eventually leads to negligible gate edge tunneling currents at higher gate bias ($V_G > 0.6$ V) in all three devices. A high gate leakage degrades the circuit performance and also causes a generation of bulk traps or electron trapping (depending on the gate voltage and direction of gate current), leading to a failure of the device.

From inversion-mode degradation trends, it can be concluded that non-STI DeMOS is significantly prone to hot-carrier degradation, compared with STI and USTI DeMOS.

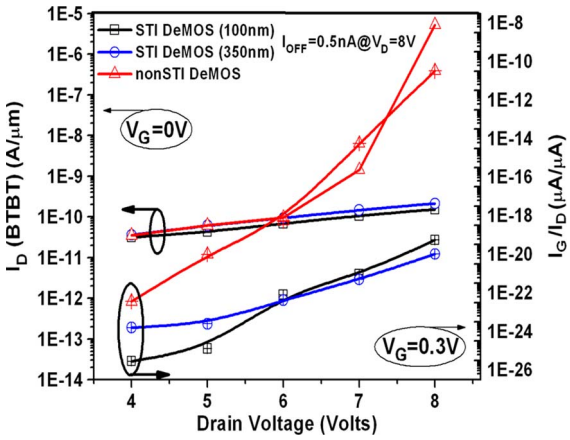


Fig. 12. Band-to-band ($I_{\mathrm{BTBT}}$) and gate edge ($I_G/I_D$) tunneling currents from MC simulations for all the different DeMOS structures.

### B. *OFF-State Degradation*

Unlike the inversion-mode hot-carrier degradation previously discussed, where hot carriers are generated by II of the source current, the source current that flows in OFF-state is only the subthreshold leakage. However, II of the subthreshold leakage alone cannot account for the total hot-carrier generation in OFF-state, and other sources such as the BTBT current need to be taken into account. OFF-state degradation was discussed in [17] and [18], and it was reported that II of the BTBT current, which was because of the high surface fields near the gate–drain edge is the dominant source of hot-carrier generation and is known to give rise to degradation that is even higher than ON-state degradation.

Fig. 12 compares the BTBT current ($V_G = 0$ V) and gate edge tunneling current with respect to drain bias ($V_G = 0.3$ V) for all the devices, which was extracted from MC simulations. STI and USTI DeMOS have a constant tunneling current for all drain biases, which shows negligible BTBT and gate edge tunneling currents in devices having STI underneath the gate-to-drain overlap. The STI helps in reducing the lateral fields near the drain. Suppressed lateral fields lead to a reduced hot-carrier generation because of the BTBT current. STI also reduces the vertical fields, which causes lower BTBT and gate edge tunneling currents. Non-STI DeMOS shows an exponential dependence of the BTBT and gate edge tunneling currents on the drain bias. At high $V_{DD}$, it shows a significantly higher current, compared with STI and USTI DeMOS, which leads to severe OFF-state degradation.

Fig. 13(a) and (b) shows 2-D hot electron and hot hole density profiles, respectively, for non-STI DeMOS. The profile was extracted from MC simulations at $V_D = 8$ V and $V_G = 0$ V. The band-to-band generation was turned on. The 2-D hot-carrier profile is in good agreement with the results discussed in [18]. The hot-carrier density peaks at the Si/$SiO_2$ interface and is close to the gate edge.

Fig. 14 shows the 1-D hot-carrier (electrons and hole) profiles for all the devices extracted 1 nm below the surface. It is clear from Fig. 14 that non-STI DeMOS has a broad distribution of hot carriers in the lateral direction and hot-carrier density of about two orders of magnitude higher, compared with STI and

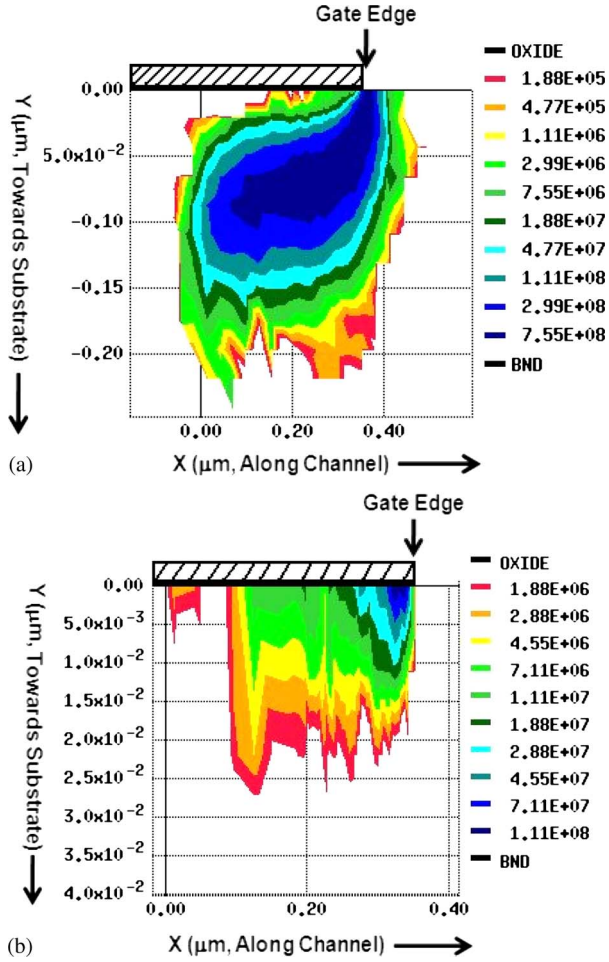


Fig. 13. (a) Two-dimensional hot electron ($E > 3.1$ eV) density profile ($\mathrm{cm}^{-3}$) extracted from MC simulation for non-STI DeMOS. (b) Two-dimensional hot hole ($E > 4.7$ eV) density ($\mathrm{cm}^{-3}$) profile extracted from MC simulation for non-STI DeMOS.

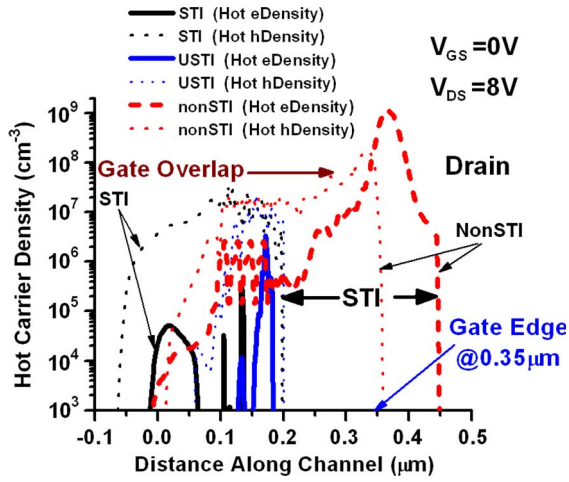


Fig. 14. One-dimensional hot-carrier density ($\mathrm{cm}^{-3}$) profile extracted from MC simulation for all DeMOS structures.

USTI DeMOS. This result is in good agreement with the results shown in Fig. 12.

In this section, we have discussed the comparison of hot-carrier generation (or eventually degradation) in USTI DeMOS with that in standard STI and nonSTI DeMOS. Results from

ON- and OFF-state degradation show that hot-carrier generation in USTI DeMOS is significantly less, compared with that in nonSTI DeMOS, and is very similar with that in STI DeMOS.

## IV. Conclusion

Non-STI DeMOS devices have a higher breakdown voltage, compared with LDDMOS, and also show an improved analog performance. However, these devices suffer from the worst gate oxide and hot-carrier reliability issues. Incorporating an STI region underneath the gate-to-drain overlap region suppresses the peak gate oxide electric field, at the cost of significantly increasing the drain resistance and degrading the turn-on characteristics of the device. We have shown, for the first time, in this work that scaling the depth of the STI underneath the gate is the key for improving both the mixed-signal and hot-carrier reliability performances of these devices. It is clear that scaling the depth of this STI region needs an extra process step. However, this additional cost can be counterbalanced by the potential saving in masks like extended lightly-doped drain formation and the silicide blocking.

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