A Novel and Robust Approach for Common Mode Feedback Using IDDG FinFET

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***Abstract*—In this paper, we propose a novel and robust approach for common mode feedback (CMFB) for a differential amplifier using independently driven double gate (IDDG) FinFET technology. The performance of a differential amplifier with and without the proposed CMFB scheme is compared using 2-D mixed mode device and circuit simulations. It is shown from extensive simulation results that it is possible to achieve a common mode rejection ratio of 90 dB with improved performance in terms of area, power, and bandwidth even in the presence of process variations. Stability analysis shows that the proposed CMFB scheme does not need any compensating network. The idea is validated using extensive mixed-mode circuit simulations on IDDG FinFET circuits in sub-45-nm node technologies.**

***Index Terms*—Common mode feedback (CMFB), FinFET, independently driven double gate (IDDG), mixed signal.**

I. Introduction

THE CMOS technology has continually pushed for the increased speed and density using shorter channel lengths. Although many performance metrics (i.e., speed, total power dissipation, etc.) have improved [1] with scaling, the control over short-channel effects (SCEs) has got worsened, leading to higher leakage currents. This necessitates introduction of novel device architectures such as FinFETs. Furthermore, mixed signal designs utilizing these technologies pose many challenges. For example, SCEs in sub-90-nm devices lead to threshold-voltage shifts, increased mismatch, and noise [2], [3]. Device mismatch has important implications on the offset voltage of op-amp and common mode rejection ratio (CMRR) of differential amplifiers [4], [5].

FinFETs are predicted as one of the best possible candidates to replace the bulk MOSFETs in the sub-45-nm regime due to their improved subthreshold slope, reduced leakage current, better short-channel performance, and compatible process flow with existing CMOS technologies [6]. It has been shown that such a device has a very high potential for analog applications due to its high value of early voltage and, hence, a large intrinsic gain [7], [8]. For future System-on-Chip solutions, it is very important to realize basic analog building blocks using FinFETs. Among analog modules, the performance of a Miller op-amp and a band-gap reference using FinFET has already been reported [9]. Most of the analog building blocks are used in wireless communication systems and hence require a low power technology that enables analog/RF and digital blocks on the same chip [10], [11].

FinFETs have a vertical fin-shaped body, perpendicular to the wafer sandwiched between front and back gates, from its two sides [12]. The fin thickness is kept below 20 nm to reduce SCE [13]. The height of the fin $(H_{\rm fin})$ is a measure of width (W) of the double-gate (DG) structure and is given by

$$W = 2H_{\rm fin}. \tag{1}$$

To increase the width, multiple fins are used between source and drain, which cause a unique phenomenon of width quantization in FinFETs [12]. Gu *et al.* [14] have proposed width quantization-aware FinFET circuit design methodologies. There are two major types of DG FinFETs, namely, simultaneously driven DG (SDDG) and independently driven DG (IDDG). SDDG has both the gates connected to each other and behaves like a three-terminal MOSFET, whereas the IDDG has two independent gates. Some SDDG structures also have a top gate, called the trigate FinFETs, whereas the top gate of IDDG FinFET is isolated by thick nitride layer. IDDG FinFETs have been proposed for dynamic threshold-voltage control and transconductance modulation. It has been shown that because of the different front-to-back gate coupling, V_T can be varied by varying the back-gate voltage $V_{\rm BG}$ [15], [16]. The change in V_T with respect to $V_{\rm BG}$ is given by [16]

$$\frac{\partial V_T}{\partial V_{\rm BG}} = \frac{-3 \times (T_{\rm oxf} + X_c/3)}{3 \times T_{\rm oxb} + (w_{\rm si} - X_c)} \tag{2}$$

where $T_{\rm oxf}$ and $T_{\rm oxb}$ are the oxide thicknesses of front and back gates, respectively, $w_{\rm si}$ is the width of silicon fin, and X_c is the distance of the charge centroid from the front gate. This unique property of IDDG FinFET can be used for dynamic threshold logic and circuits [18]. So far, a few research groups [16], [18], [19] have looked into the novel realization of analog circuit modules using IDDG FinFET transistors [20], [21]. In this paper, for the first time, a novel common mode feedback (CMFB) scheme is proposed, utilizing the IDDG operation of FinFETs.

Differential amplifiers with CMFB have been reported in processes with feature size below 90 nm [28]. Fully differential

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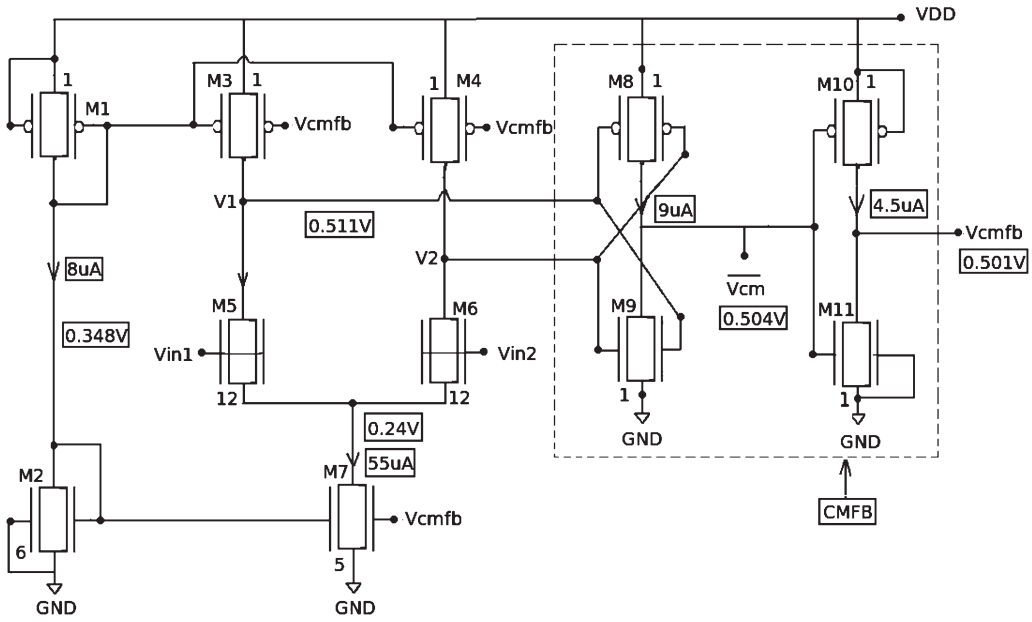


Fig. 1. Proposed CMFB circuit scheme. Number of fins is shown for each transistor. The configuration shown in box is used for suppressing CM variations.

operational transconductance amplifier (OTA), reported in [28], has been designed and simulated in 45-nm bulk and 45-nm FinFET technologies with 1-V supply voltage. This OTA has a gain-bandwidth product of 400 MHz. The CMFB circuit reported in [28] needs a reference voltage. Another work demonstrates fabrication of a GSM receiver front end in conventional 65-nm digital CMOS process [29]. The CMFB circuit used in the low noise amplifier (LNA) is a conventional reference-based CMFB. The operating frequency range of the reported LNA is GSM band. The folded cascode amplifier with embedded CMFB, reported in [30], uses dynamic threshold MOS technique for low-voltage operation in 0.18-μm bulk CMOS technology. Two PMOS transistors act as two resistors for detecting common-mode (CM) voltage [30]. This voltage is fed back to the body terminal of the tail current source used to bias the folded cascode amplifier [30]. Measured and simulated CMRRs are 48.4 and 51.2 dB only. Gain bandwidth product of the amplifier is 11.2 MHz [30].

This paper is arranged in the following way. The proposed circuit is described in Section II. The realization of IDDG FinFET for circuit simulation is discussed in Section III. Section IV emphasizes on the circuit simulation results, while Section V summarizes the important findings from this paper.

II. Proposed Scheme

A CMFB circuit stabilizes CM voltages for fully differential analog systems by means of adjusting the CM currents. In a conventional CMFB circuit, the CM output voltage at two differential terminals is averaged to get a CM voltage $(V_{\rm cm})$, which is compared with a reference voltage $(V_{\rm Ref})$. The output of the comparator is then used to generate CM current, which eventually controls the CM output voltage.

In this paper, a novel architecture for CMFB using IDDG FinFET, which facilitates high bandwidth differential amplifiers is shown. Fig. 1 shows a fully differential amplifier with proposed CMFB circuit realized using 32-nm IDDG FinFET transistors. The arrangement shown in the box is used for suppressing CM variations.

Transistors M1 and M2 are used to generate bias currents of M3, M4, and M7 of the differential amplifier. It should be noted that biasing circuit is not limited to the configuration shown in Fig. 1 and that other circuits can be used for that purpose. V_1 and V_2 are output terminals of differential amplifier, which are biased at $V_{\rm dd/2}$, i.e., 0.5 V. CM voltage $(V_{\rm cm})$ is generated using M8 and M9. This is because small signal drain current of M8 (or M9) is proportional to the CM of small signal voltages of front and back gates of M8 (or M9). If the CM of V_1 and V_2 increases (or decreases), output voltage of M8 (or M9) will decrease (or increase). Cross-coupled arrangement of M8 and M9 makes $V_{\rm cm}$ insensitive to any differential change in V_1 and V_2.

M10 and M11 comprise a simple inverter to invert the common-mode voltage, generated by M8 and M9, and to produce $V_{\rm cmfb}$, the CMFB voltage. $V_{\rm cmfb}$ is in phase with the CM of V_1 and V_2, which is fed back to the back gate of M3–M4 and M7. As V_1 and V_2 increase (decrease), $V_{\rm cmfb}$ increases (decreases), and hence, the current through M3 and M4 will decrease (increase), which will decrease (increase) the CM of V_1 and V_2. Since $V_{\rm cmfb}$ is also fed to M7, it causes an increase (decrease) in the drain current of M7, leading to a decrease (increase) in V_1 and V_2.

The purpose of connecting the M1, M2, M10, and M11 transistor back gates to the supply level is to reduce the power. M1 and M2 provide the reference current for biasing transistors in the circuit. This reference current is a function of "W/L" of M1 and M2. For a given value of $(W/L)_{M2}/(W/L)_{M1}$, one can reduce the reference current by lowering the effective $(W/L)_{M2}$. Since M2 is already a single-fin device, by connecting the M2 back gate to the $V_{\rm dd}$, its effective W is reduced. Accordingly, the back gate of M1 is connected to $V_{\rm ss}$ to keep the ratio of the aspect ratios of M1 and M2 constant.

TABLE I
NUMBER OF FINS IN VARIOUS TRANSISTORS

Transistors	No of Fins
M1, M3, M4	1
M8, M9, M10, M11	1
M5, M6	12
M2	6
M7	5

To reduce bias current in the branch of M10 and M11, their effective width is reduced by a factor of 50% by connecting their back gate to the supply levels. Overall, loop gain of CMFB will not be affected by this connection. We have already simulated the circuit by keeping M1, M2, M10, and M11 in SDDG mode, and no difference has been observed except power increase.

Size of transistors M2 and M7 is determined according to the bias current considered for the differential amplifier. Value of this bias current depends on the required bandwidth and power constraints. Effective aspect ratio of M7 is made larger than that of M2 to reduce power consumption. In this paper, the effective aspect ratio of M7 and M2 are five and three, respectively. The aspect ratio of transistors M5 and M6 is determined based on the minimum required voltage gain of the amplifier.

It is worth to mention here that the width of all transistors was chosen so as to make it an integer multiple of $2H_{\rm fin}$, where $H_{\rm fin}$ is the fin height. Therefore, no rounding of widths is required. After calculating the required widths, the number of fins is determined as per the following relation:

$$W = n * 2H_{\rm fin} \tag{3}$$

where n is the number of fins (which is an integer number) and $H_{\rm fin}$ is the height of the fin. Fin height was taken as 65 nm, which is reported in many references [22], [23]. Details regarding the number of fins are provided in Table I.

Here, $V_{\rm cmfb}$ itself gets biased since there are two feedback paths from $V_{\rm cmfb}$ to the biasing transistors M3–M4 and M7. It is clear from the circuit that as $V_{\rm cmfb}$ drifts, I(M3), I(M4) and I(M7) try to move in opposite directions. By considering that all transistors are in strong inversion, relations (4) and (5) show how $V_{\rm cmfb}$ is biased at a particular value.

$$I_{\rm M7} = I_{\rm M4} + I_{\rm M3} \tag{4}$$

or

$$\frac{1}{2}\beta_n(V_{\rm cmfb} - V_{\rm ss} - V_{\rm tn})^2 = \beta_p(V_{\rm dd} - V_{\rm cmfb} - V_{\rm tp})^2 \tag{5}$$

where $V_{\rm tp}$ and $V_{\rm tn}$ are the threshold voltages for PMOS and NMOS, respectively. Similarly, as discussed earlier, variation in CM of V_1 and V_2 changes $V_{\rm cmfb}$ in the same phase, thereby stabilizing $V_{\rm cmfb}$. Hence, the robustness of the circuit is proved. If SCEs are not negligible or if some of the transistors of the input differential pair operate in weak inversion, (5) will need to be modified. However, the dc level of $V_{\rm cmfb}$ will get set properly to the solution of the modified equation.

The proposed circuit can also be designed using SDDG transistors, but it will have the following drawbacks.

1) In case of SDDG, we need more number of transistors to cancel out the differential-mode signals and get the CM. This is because SDDG is not capable of canceling out the differential-mode signals, and we need at least two more transistors to achieve the differential-mode rejection. In IDDG mode, transistors M8 and M9 simply accomplish this task.
2) The CMFB configuration shown in Fig. 1 is insensitive to differential changes. Common fin between the front and back gates of IDDG structure helps both sides of IDDG structure remain identical even in the presence of process variations as compared with two SDDG transistors with their drain and source connected to each other. Therefore, in the case of M8 and M9 in Fig. 1, differential-mode small signal current at the front and back channels of M8 or M9 will have 180° phase difference. As a result, differential-mode drain and source currents of M8 or M9 will be zero in the differential mode. This completely cancels out the differential signals. This is not easily achievable by two parallel SDDG transistors instead of single IDDG transistor.

The proposed circuit structure for CMFB uses very few transistors as compared with the conventional ones and hence occupies lesser layout area. Implementing the same circuit using SDDG transistors will need 16 transistors. This means that the area overhead compared with IDDG case will be around 40%. This scheme can be used to design a complete op-amp having very high bandwidth and CM rejection capability for mixed signal applications at sub-45-nm technologies.

III. DEVICE REALIZATION

Fig. 2 shows the top view of a single-fin IDDG FinFET realized using *Sentaurus Device Editor* [24]. The device structure is IDDG having two gates (front and back gates). Device dimensions and doping levels are given in Table II both for the PMOS and NMOS transistors.

The channel length used here is 32 nm, and fin thickness is kept approximately Lg/2, i.e., 15 nm to control the SCEs. The fin is undoped having a doping density of 1×10^{15} cm^{-3}. The intrinsic fin helps in reducing the random dopant fluctuations [25]. The important device dimensions are summarized in Table II.

The device/mixed-mode circuit simulations are performed using *Sentaurus TCAD tools* [26]. Calibrated drift-diffusion models are used. For the mobility, we have used the "Lombardi" model with calibrated model parameters [22], [23]. The channel in FinFET is on the sidewall of the fin that lies on (110) plane if the device is fabricated on a wafer having orientation (100). Due to dissimilar physical properties of effective mass along various axes, hole mobility in FinFET gets enhanced, and

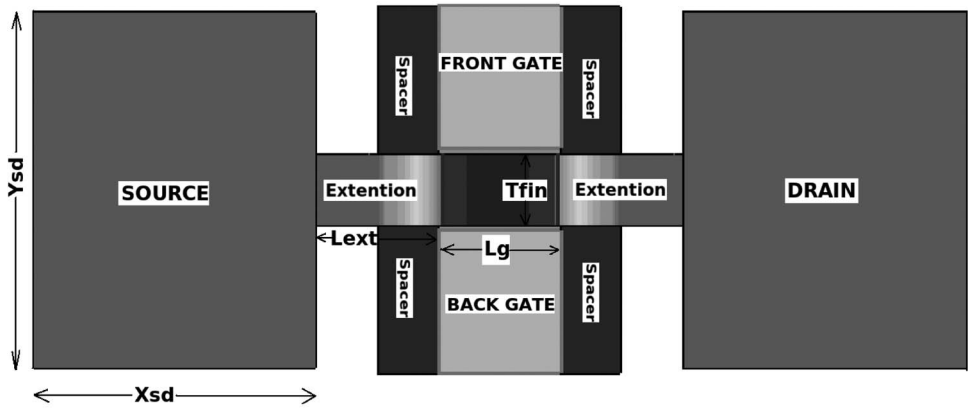


Fig. 2. Realized IDDG FinFET structure. Device dimensions are given in Table II. Structure and dimension are the same for NMOS and PMOS.

TABLE II
DEVICE DIMENSIONS AND DOPINGS (SAME FOR NMOS AND PMOS)

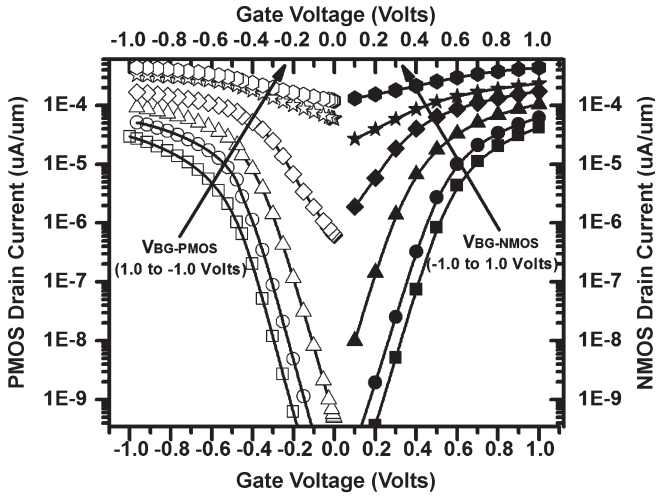
Attributes	Values
L_g	32nm
T_{Fin}	15nm
T_{OX} (EOT)	1.1nm
L_{ext}	32nm
Spacers	16nm
X_{sd} and Y_{sd}	75nm
Fin Doping	$1x10^{15}$ cm^{-3}
S/D Doping	$1x10^{20}$ cm^{-3}
Extension Doping	$1x10^{19}$ cm^{-3}

TABLE III
DEVICE SPECIFICATIONS

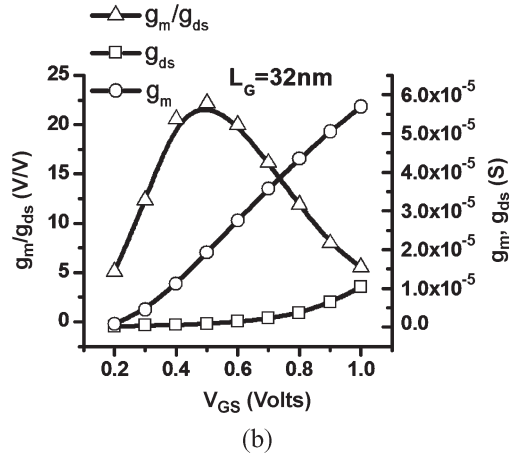
Attributes	NMOS	PMOS
ϕ_m	4.4eV	4.84eV
V_T	0.22V	-0.22V
I_{ON}	437μA/μm	442μA/μm
I_{OFF}	9nA/μm	9nA/μm

electron mobility gets degraded as compared with conventional planar devices with (100) surface orientation [27]. Sidewall roughness, stress, and strain also affect the mobility. Since the default model parameters used in device simulator are for (100) plane, mobility model parameters have been modified for (110) plane [22]. The contact resistivity value chosen for the simulations is $1.45 \times 10^{-7}\ \Omega \cdot \text{cm}^2$. Instead of using a polysilicon gate, metal gate is used, and threshold voltages are optimized by modifying the metal work function as listed in Table III. All internal parasitic capacitances of the devices and series resistances are taken into account for the device/mixed-mode circuit simulations.

Simulated I_D–V_G for various backgate voltages both for NMOS and PMOS is shown in Fig. 3(a). The achieved on and off currents and V_T are listed in Table III. Analog figures of merit, i.e., gm, gds, and gm/gds for devices with a channel length of 32 nm, used in the circuit, are shown in Fig. 3(b).



(a)



(b)

Fig. 3. (a) I_D–V_G plots for NMOS and PMOS with 32-nm channel length. (b) gm, gds, and gm/gds plots for NMOS with 32-nm channel length.

IV. SIMULATION RESULTS

This section presents performance and robustness of the CMFB circuit and the differential amplifier. Achieved

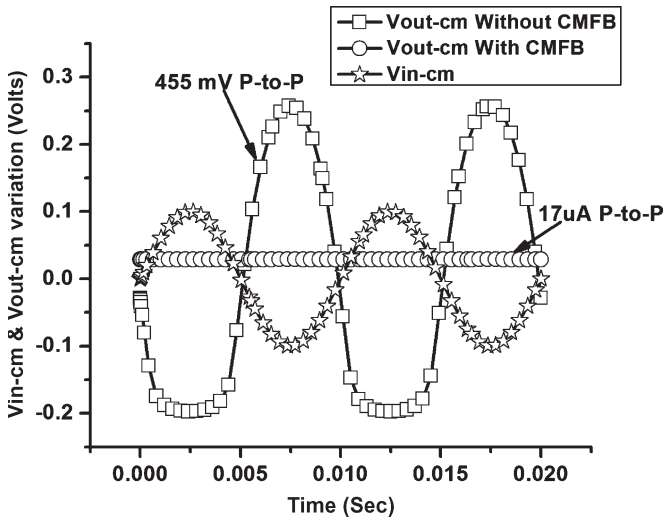


Fig. 4. Comparison of CM performance of the differential amplifier with and without the proposed CMFB circuit.

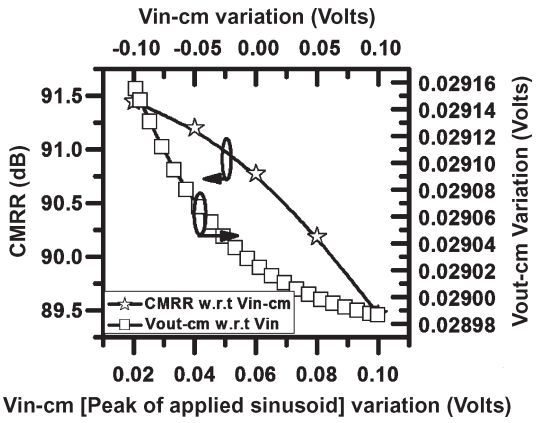


Fig. 5. Variation in $V_{\mathrm{out-cm}}$ with respect to (w.r.t.) variation in $V_{\mathrm{in-cm}}$ (right Y-axis) and CMRR variation w.r.t $V_{\mathrm{in-cm}}$ variation (left Y-axis). Here, the $V_{\mathrm{in-cm}}$ is the peak of CM sinusoid applied to the input of differential amplifier.

performance will be compared with state-of-the-art specifications reported to date. The circuit has been simulated using 2-D mixed mode simulation in *Sentaurus Device* [26]. The nodes V_{in1}, V_{in2}, V_1, V_2, V_{cm}, and V_{cmfb} are biased at $V_{\mathrm{dd}/2}$, i.e., 0.5 V. The exact values of voltages and currents are shown in Fig. 1. Total current drawn from the supply was 77 μA.

A. CMFB Performance

The performance of differential amplifier without using any CMFB and with the proposed scheme has been compared. Fig. 4 shows the CMRR. A CM sinusoidal signal with a peak-to-peak (p-to-p) value of 0.2 V was applied to the inputs. In case of no CMFB circuit, CM signal was amplified to 455 mV p-to-p. However, it decreases to 17-μV p-to-p when the proposed scheme for CMFB was used; this led to a CM attenuation of 62 dB and a CMRR of 90 dB.

Fig. 5 shows the dc output CM variation by varying the dc input CM voltage. It was observed that the output CM variation

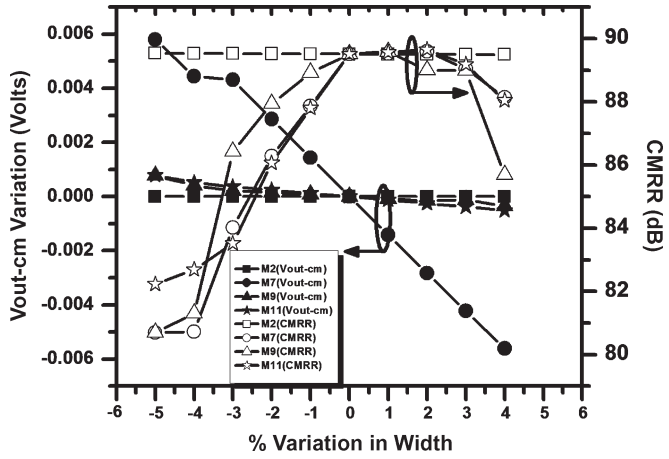


Fig. 6. $V_{\mathrm{out-cm}}$ and CMRR variation w.r.t. percentage change in the width of individual transistors.

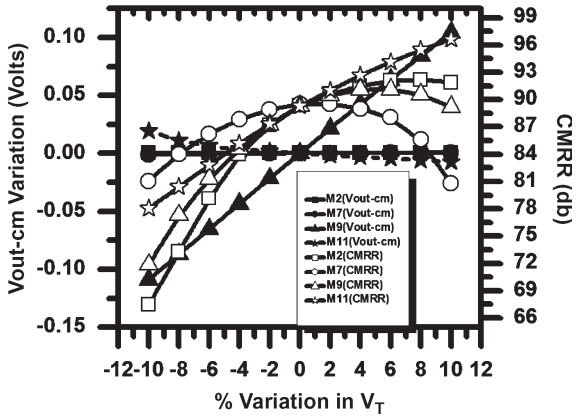


Fig. 7. $V_{\mathrm{out-cm}}$ and CMRR variation w.r.t. percentage change in the threshold voltage of individual transistors.

was not more than 17 μV for a $\pm$0.1-V CM voltage variation at the input.

The variation of CMRR with $V_{\mathrm{in-cm}}$ is also shown in Fig. 5. The CM gain was found by applying a CM sinusoidal input of 100-mV peak and by observing the output CM variation. $V_{\mathrm{in-cm}}$ is the peak voltage of CM sinusoidal signal applied at the input to find CMRR. High value of CMRR is due to high gain of the CMFB circuit. Along with high gain, stability of CMFB is also required, which will be discussed later in this paper.

B. Effect of Process and Temperature Variations on the CM Performance

Stability of dc CM voltage in the presence of process variations was also studied. We studied for a $\pm$10% variation in threshold voltage, $\pm$5% variation in width, and $\pm$10% variation in the electron mobility of M2, M9, M11, and M7. Variations of output dc CM voltage and CMRR with variation of width, mobility, and threshold voltage are shown in Figs. 6, 7, and 8, respectively. In the variability analysis, the parameter of only one transistor is varied at one time.

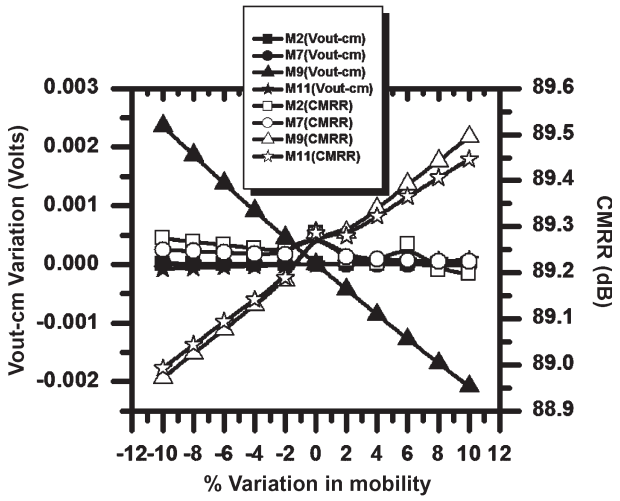


Fig. 8. $V_{\mathrm{out-cm}}$ and CMRR variation w.r.t. percentage change in the mobility of individual transistors.

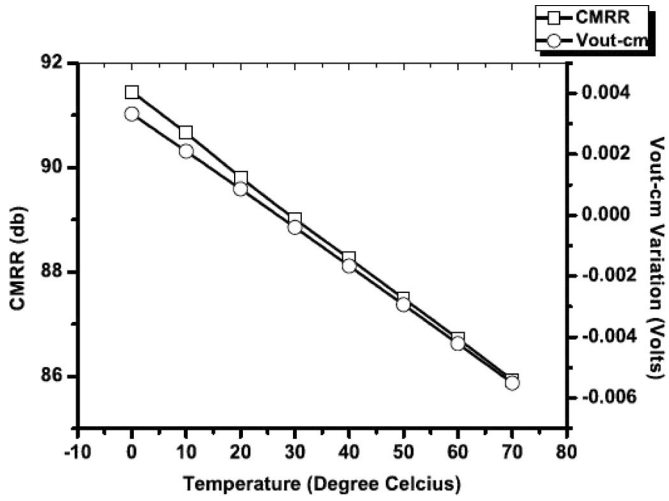


Fig. 9. $V_{\mathrm{out-cm}}$ and CMRR variation w.r.t. change in the temperature of the circuit.

Fig. 6 shows that the variation of width of M2, M7, and M11 has an insignificant impact on the output dc CM voltage, which is in microvolts. Varying the width of M9 by $\pm 5\%$ drifts the output CM voltage by ± 7 mV, which is still in the acceptable limits. The variation in the width of M2 does not affect the CM performance of the circuit, but the variation in widths of M7, M9, and M11 changes the loop gain of CMFB and hence changes the CMRR. It is clear from Fig. 6 that degradation in CMRR is slightly higher for a negative variation as compared with the positive variation in width. The minimum CMRR achieved was 81 dB, which still shows a very high CM performance.

Results for $\pm 10\%$ variation in threshold voltage (V_T) are shown in Fig. 7. The minimum CMRR achieved from max variation in V_T of M2 and M7 was 80 dB. The plot shows that positive variation in V_T of M7, M9, and M11 improves the CMRR up to 97 dB. This improvement results from improvement in the loop gain of the feedback path, which gives a better CM rejection performance. Consequently, the negative variation in the threshold voltage of M9 and M11 decreases the CMRR down to 70 dB.

Asymmetry in CMRR variation with respect to positive and negative variations of parameters originates from the asymmetric variation of loop gain in the CMFB circuit and the variation of differential-mode gain in the differential amplifier. These variations are not necessarily symmetric. For example, the loop gain is controlled by the voltage gain of two amplifiers composed of transistors M8, M9, M10, and M11. These amplifiers have been realized using inverters and hence exhibit the maximum gain at their switching point. Ideally, transistors M8–M11 are sized in such a way that the switching point at the middle value of supply level is kept. However, there is a few millivolt difference between dc values of V_1, V_2, $\overline{V_{\mathrm{cm}}}$ (drain of M8 and M9), and V_{cmfb} in Fig. 1. This is because widths are sized in a quantized manner in FinFETs, and hence, there is a small imbalance in the amplifier characteristics. This small imbalance makes CMRR degradation different for positive and negative variations of the width or V_T.

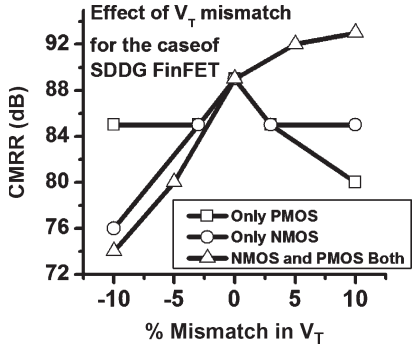


Fig. 10. Effect of V_T mismatch on CMRR for the case of SDDG FinFETs.

Effect of mobility variation is also studied, as shown in Fig. 8. It can be seen that CMRR is insensitive to mobility variations. Intrinsic or low-doped fins lead to high mobility of the carriers in the channel as well as to the lower variations. Fig. 9 shows that the temperature variation does not influence CMRR and $V_{\mathrm{out-cm}}$ significantly.

To quantify the amount of CMRR degradation, an SDDG version of the circuit was simulated, and variation of CMRR with respect to the percentage of V_T mismatch between two SDDG transistors used for each of M8 (PMOS) and M9 (NMOS) was observed. Fig. 10 shows the simulation results of CMRR degradation. For example, for the case of -6 mV (2.7%) mismatch between V_T of SDDG devices used for M8 and M9, CMRR reduces by 5 dB. In Fig. 10, CMRR increases for the case of increasing absolute value of threshold-voltage mismatch in both PMOS and NMOS transistors. This is because bias current of M8–M9 branch reduces as a result of this mismatch, and hence, CM loop gain increases, which leads to a higher CMRR in the case of positive V_T mismatch. It should be noted that CMRR degradation due to mismatch in SDDG devices is not the only factor which gives preference to IDDG implementation of the circuit. By replacing the IDDG devices with SDDG devices, the dc current in M8–M9 branch was doubled, and also, the planar area was increased due to the addition of one more FinFET for each transistor.

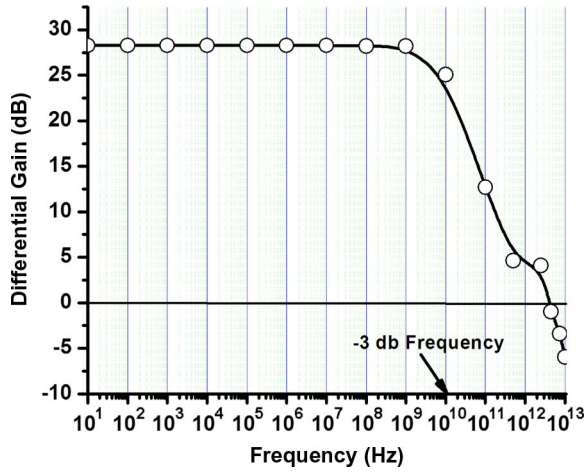


Fig. 11. Frequency response of the differential amplifier.

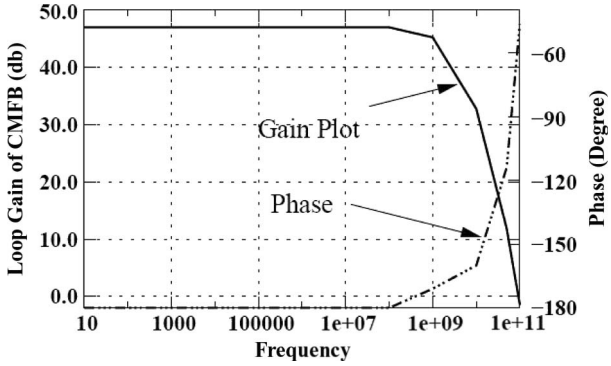


Fig. 12. Open-loop frequency response of CMFB circuit for stability analysis.

C. Frequency Response

Fig. 11 shows the frequency response of the differential amplifier. The −3-dB bandwidth of the differential amplifier was 10 GHz with a differential gain of 28 dB, which shows very high performance for high-bandwidth analog/mixed signal applications. All parasitic capacitances, including gate area, gate overlap capacitances through spacer, and source/drain capacitances, have been taken into account. These capacitances constitute the main component of parasitic capacitances present in the circuit because all the circuit nodes are connected to the gate terminal of FinFETs except the drain of M7 which is not affected by the differential-mode signals.

Stability of CMFB circuit was also analyzed. Fig. 12 shows that CMFB has a very high phase margin, which demonstrates a highly stable feedback circuit without using any compensating network.

D. Robustness

Fig. 13 shows the variation of ±0.1 dB in differential gain for a ±10% variation in mobility of all transistors in the circuits, i.e., M1–M11. The mobility of all the transistors is varied simultaneously. Similarly, it is also shown in Fig. 13 that the temperature variation causes a minimal change in the differential performance. For a temperature range of operation, i.e., 0 °C–70 °C, the differential gain varies from 29.5 to 26 dB.

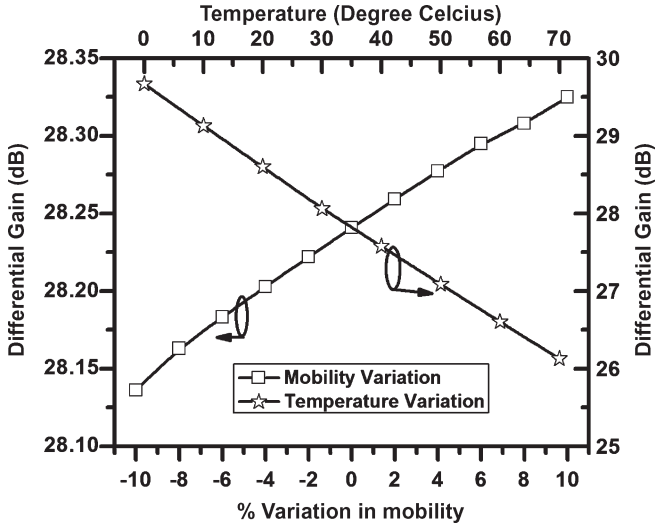


Fig. 13. Effect of temperature and mobility variation on differential gain of the amplifier. A slight variation in differential gain proves the robustness of the circuit.

V. Conclusion

In this paper, a novel CMFB circuit using IDDG transistors is presented and validated using well-calibrated mixed-mode TCAD simulations. It has been shown that by the use of back-gate bias in IDDG FinFETs, novel circuit configurations are possible that utilize fewer number of transistors and lower power and area compared with the identical circuits designed using the SDDG devices. A single IDDG transistor can operate as two transistors with common source and drain terminals. The inherent symmetry in the front and back gates of IDDG transistors can be fully exploited to improve the performance of CMFB circuits (because of the insensitivity to differential inputs at the front and back gates) as has been demonstrated in this paper.

The proposed IDDG FinFET circuit in this paper shows the best case CMRR of 90 dB (and the worst case CMRR of 70 dB), a differential gain of 28 dB with a 77-μW power dissipation, and a 10-GHz bandwidth.

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