A Novel High Voltage Drain Extended FinFET SCR for SoC Applications

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***Abstract*— In this work, physical insights into missing SCR action in High Voltage drain extended FinFET SCR is developed using detailed 3D TCAD simulations. The 3D TCAD simulations revealed that the missing SCR action in STI-DeFinFET SCR is due to the weak bipolar strength associated with the PNP corresponding to the anode (P+) contact. A novel Dual-Fin STI DeFinFET SCR architecture is revealed to address this roadblock and achieve SCR action in these devices, which offered a failure threshold 3X times higher than the conventional device. Furthermore, to investigate the filament behavior, a 64-Fin Dual-Fin STI DeFinFET SCR is simulated, revealing severe filament driven low current failure in these devices. Silicide blocking and well-implant engineering were found to improve power scalability issues in these devices.**

***Index Terms*—Electrostatic discharge, Drain-extended FinFET (DeFinFET), SoC, Silicon Controlled Rectifiers, Technology Computer Aided Design (TCAD).**

I. INTRODUCTION

Bulk FinFETs have replaced planar MOSFET for technology scaling beyond 22nm technology nodes. FinFETs offer lower leakage and, thus, a higher performance due to their superior electrostatic control. However, due to reduced silicon volume and Fin-like geometry, they are vulnerable to ESD-like stress. Therefore, a detailed study of the failure mechanisms in various Fin-based devices under ESD stress is critical. This work attempts to understand failure in high voltage Drain-Extended FinFETs.

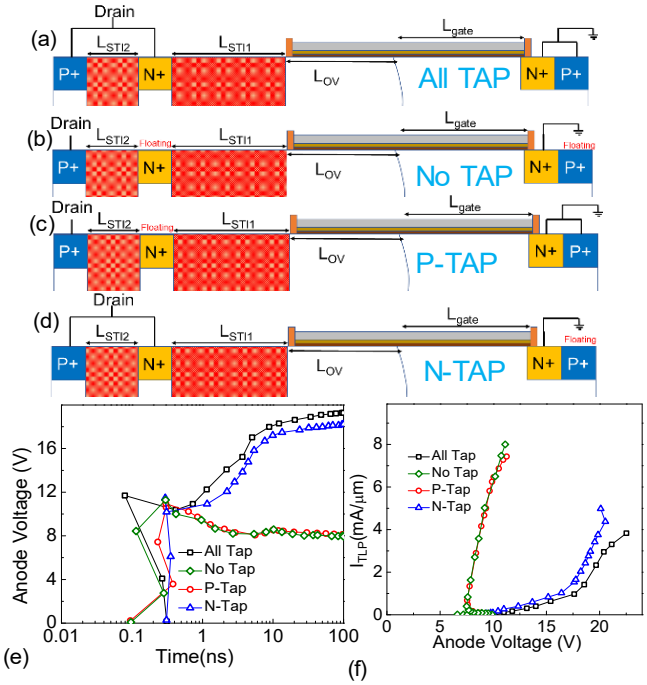

Fig. 2: (a)-(d) Configuration of STI-DeFinFET SCR explored to study the cause of missing SCR action. (e) Transient anode Voltage for an injected current of 2mA/um showing the presence of SCR action only when both the taps are removed (**Fig. 2b**) and when only P-Tap is missing SCR action can be attributed to weak PNP turn-on. Therefore, Improving PNP efficiency alone can increase I_{T2} by introducing an SCR action

For high voltage devices in SoC application, Drain-Extended FinFETs are preferred over cascaded ggFinFETs [1]. However, due to the high drift length, Drain-Extended

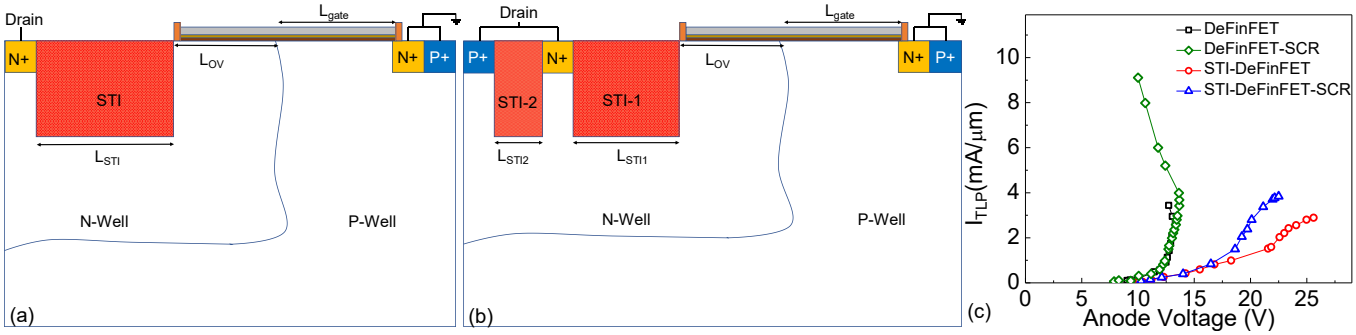

Fig. 1: Schematic of (a) STI-DeFinFET and (b) STI-DeFinFET SCR. (c) TLP I-V of these devices along with the variant of these devices without STI in the drain extended region. Introducing a P+ in the drain region of the DeFinFET was found to improve its It2 by two folds. However, such an approach in STI-DeFinFET failed to yield any significant improvement in the failure threshold.

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FinFETs have poor ESD robustness. Drain-Extended FinFET SCR's with an extra P+ implant (**Fig. 1a**) in the drift region, which is a concept derived from planar nodes [2]-[3], used to address this issue [4]-[5]. However, such an approach failed to improve the ESD robustness of STI type Drain-Extended FinFETs (**Fig. 1b-c**). In this work, physical insights towards the absence of SCR turn-on in STI DeFinFET SCR is developed. And using these developed insights, a modified device is proposed, which offered a 3.5x improvement in failure threshold.

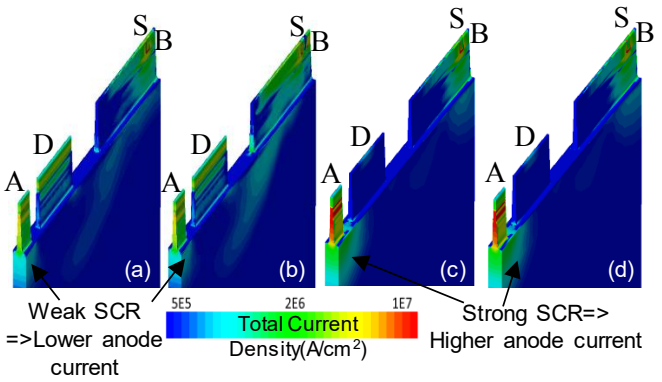

Fig. 3: (a)-(d) Current density contour plotted for an injected TLP current of 2mA/um at 100ns for all four configurations. Removing N-Tap/Drain (i.e. either without any TAP or with P-Tap only) was found to turn-on the SCR (Higher anode to cathode conduction). This weak pnp turn-on can be attributed to high anode to junction distance.

Furthermore, a 64-Fin device is simulated to understand the filament dynamics of this device under ESD stress. Finally, design guidelines are developed to engineer these devices for better power scalability. The injected TLP current has a 10ns rise time and a 100ns pulse width. Each point in all the TLP-IV curves is extracted by averaging the voltage across the device between 60ns and 90ns. Furthermore, the simulation setup (including calibration and physics models used) used in this study is the same as [4].

II. Physical Insights Into Missing SCR Action

The devices were tested under four unique configurations to understand the SCR action (a) With all (/both) (Fig. 2a) (b) Without any taps (Fig. 2b) (c) With P-Tap only (Fig. 2c) (d) With N-Tap only (Fig. 2d). Fig. 2e and Fig. 2f show the TLP-IV and transient terminal voltage of these devices under ESD stress, respectively. The devices with both taps and only N-Tap do not have any SCR turn-on (Fig. 3a-b), resulting in the absence of snapback characteristic in their respective TLP-IVs (Fig. 2e). However, the devices without either tap and those with only P-Tap show a strong SCR turn-on (Fig. 3c-d) and, therefore, the presence of snapback characteristics in their TLP-IVs (Fig. 2f). In devices without P-Tap (N-Tap), the bipolar efficiency of the NPN (PNP) associated with the SCR is maximized. Therefore, increasing the bipolar efficiency of NPN (With P-Tap only) associated with the SCR does not seem to affect the device's snapback characteristics. Improving the bipolar efficiency of PNP (With N-tap only) improves the SCR turn-on and, therefore, better failure threshold. However, such a device without N-Tap is not practical since N-Tap acts as the device's drain contact. In the next section, a new architecture is revealed to improve PNP's bipolar strength associated with the SCR.

III. Dual-Fin STI DeFinFET SCR

The emitter to collector distance needs to be decreased to improve bipolar strength without changing well doping and silicide blocking length. In the conventional single-fin device, the total emitter to collector junction distance is equal to $L_{ov}+L_{STI1}+L_{Drain}+L_{STI2}$. In the proposed dual fin architecture (Fig. 4a), the anode and the drain contact are parallel. This reduces the effective emitter to collector contact distance of the PNP associated with the SCR to $L_{ov}+L_{STI}$. Therefore, resulting in a better SCR turn-on and a failure current 3.5X times the conventional device (Fig. 4c). DC simulation was performed on this device with and without the P+ contact. DC

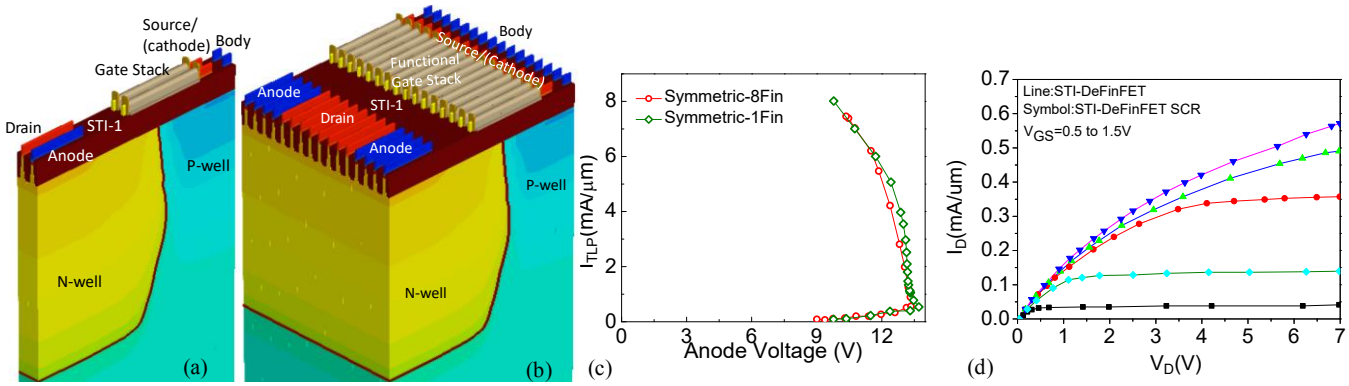

Fig. 4: Isometric view of (a) Dual-Fin STI-DeFinFET SCR (b)A unit cell of 8 FET-Dual Fin STI-DeFinFET SCR.(c) Simulated TLP-IV of **Fig. 4a** and **Fig. 4b** showing an improvement of 3X in failure current compared to a conventional device which is the result of a strong SCR turn-on induced snapback. (d) DC-IV showing that the SCR does not get triggered in the normal transistor operation regime thereby the transistor operation remains unaltered by the SCR(P+) implant. This improvement is due to reduced anode to well distance as a result of dual finger placement at the drain side.

simulation (Fig. 4d) was performed on this device with and without the P+ implant. These simulations revealed that the SCR formed does not interfere with the DC transistor operation.

Despite these devices offering a superior ESD characteristic, there might be some difficulties doping each fin of a device with a more extensive array separately. An 8-Fin Unit-cell variant of the Dual-Fin STI DeFinFET is shown in Fig. 4b. Here the doping on the drain side is kept constant in blocks of 8-Fins. This device's failure current reduces to 15% of the previous structure, which is still 3X times that of the conventional device. A 64-Fin Dual-Fin STI DeFinFET SCR is simulated to understand these devices' filament behavior under ESD stress in the next section.

IV. Power Scalability Issues and Filament Engineering

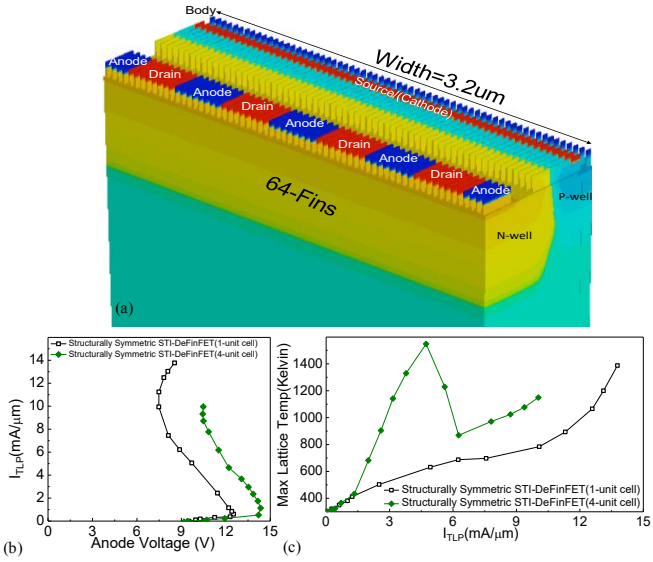

Fig. 5: (a) Schematic of 64-Fin device. Simulated (b) TLP-IV and (c) TLP-IT of Fig4(b) for a single unit cell structure (16 Fin) and a 4 Unit-cell structure (64 Fin) showing power scalability issues, resulting in the device failing at lower injected current and surviving at higher injected current. A 64 Fin device was simulated to reproduce the filament behavior in these devices.

Fig. 5a depicts the schematic of a 64-Fin Dual-Fin STI DeFinFET SCR simulated to understand filament behavior. **Fig. 5b** and **Fig. 5c** show the TLP-IV and TLP-IT respectively of a 64-Fin Dual-Fin STI DeFinFET SCR (**Fig. 5a**) and a 16-Fin Dual-Fin STI DeFinFET SCR (Fig. 4b). There is a significant difference between the TLP-IV of a 16-Fin device and a 64-Fin one. This difference can be attributed to the filament behavior of the device in a multi-Fin arrangement. Furthermore, the TLP-IT of the device shows that the 64-Fin device fails at lower injected currents(4.7mA/um) around the snapback and survives higher injected(10mA/um) currents. This deviation in the device's behavior from the power-law (Wunch-bell curve) is referred to as power scalability issue. The power scalability issue

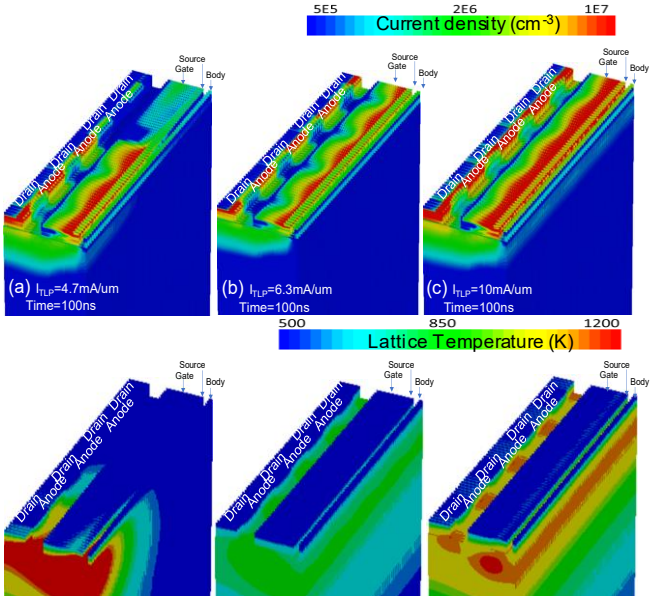

Fig. 6: (a)-(c), (d)-(f) Conduction current density and Lattice temperature contour respectively plotted for a 64 Fin Dual Fin STI-DeFinFET SCR showing current filamentation for low current resulting in a highly concentrated hot-spot and as higher current is injected the hot spot relaxes as the current spreads across the various fins as more FinFET's are turned-on for higher injected current (6.3,10 mA/um)

arises due to current filament formation in High-Voltage MOS SCRs. Therefore, they are present only in a 64-Fin device and not any devices with lower fins (16- & 2- Fins) because they cannot capture the filament behavior.

Fig. 6a-c and **Fig. 6d-f** shows conduction current density and maximum lattice temperature respective of **Fig. 5a** extracted for different TLP injected current. At lower injected current around the snapback region where the device enters the thermal failure region, the current conduction is localized to a few fins (**Fig. 6a**), resulting in a very concentrated hotspot (**Fig. 6d**). As the injected current is increased, more impact ionization generated carriers are generated to turn-on other sections of the SCR, resulting in filament spreading (**Fig. 6b-c**). Therefore, the hotspot spreads across the device width (**Fig. 6e-f**), relaxing the maximum lattice temperature. The poor power scalability characteristic in these devices is due to a weak SCR action. This weak SCR action can be primarily attributed to the weak bipolar strength of the NPN associated with the intrinsic STI-DeFinFET. Therefore, to improve power scalability, the overall SCR strength of the device needs to be improved. To further enhance the overall SCR strength, two engineering techniques are discussed in this work.

A. N-Well implant engineering: N-Well implant engineering: **Fig. 7a** shows the N-Well doping variations explored in this work. DC simulations were first performed to ensure that these variations in Well doping don't result in SCR trigger in normal transistor operation. Decreasing N-Well doping improves the bipolar strength of the PNP associated with the SCR by increasing the base resistance. This overall

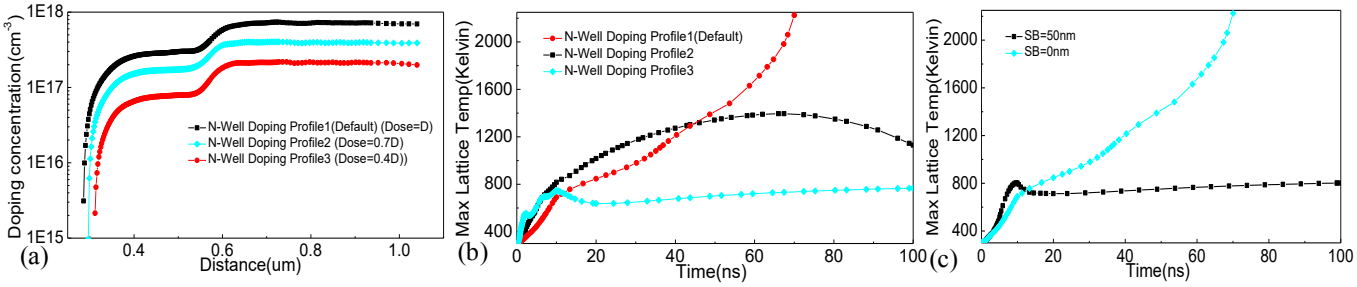

Fig. 7: (a) N-Well doping profile variations explored along the line X-X' in Fig. 4(b) for a 64-fin structure. (b) Transient lattice temperature showing current filament induced thermal runaway in the device with default doping and power scalability improving as the N-Well doping profile in changed. (c) Transient maximum lattice temperature for variation in silicide (@I_{TLP}=4.7mA/um).

improvement in SCR strength improves the power scalability issue, as seen in **Fig. 7b**.

B. Silicide blocking: Silicide blocking on the anode (Drain) side increases the diffusion length in the PNP's emitter region. They also increase the N-Tap contact resistance (Drain), decreasing base recombination and therefore better PNP bipolar efficiency. This overall improvement in SCR strength results in a better power scalability as shown in **Fig. 7c**. On one hand, silicide blocking increases the overall SCR strength, and, on the other hand, it also increases the anode contact resistance. Therefore, if the silicide blocking is increased beyond an optimum distance, the increased contact resistance will significantly decrease the device's final failure threshold. DC simulation performed on the devices with both the engineering technique showed less than 5 percent deviation from the intrinsic DC characteristics. This confirmed that these techniques would not interfere significantly with the normal operation regime.

V. Conclusion

The absence of SCR action in STI-DeFinFET SCR is due to the weak bipolar strength of the PNP. The proposed Dual-Fin STI-DeFinFET SCR improved PNP's bipolar strength by decreasing the emitter to base-collector junction distance. Therefore, the newly proposed device offered a failure threshold of 3.5X the conventional device due to an SCR driven snapback in their TLP-IV. Furthermore, a 16-Fin Unit cell variant of the Dual-Fin STI DeFinFET SCR was revealed to make the doping easier. A 64-Fin Dual-Fin STI DeFinFET SCR simulated was found to suffer a filament driven low current failure. However, these devices survived high injected current. This power scalability problem arises due to the weak bipolar strength of NPN associated with the intrinsic STI-DeFinFET. N-Well implant engineering and silicide blocking improved this power scalability issue.

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