Peculiar Current Instabilities & Failure Mechanism in Vertically Stacked Nanosheet ggN-FET

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***Abstract*— The behavior of gate grounded vertically stacked nanosheet N-FET (ggNFET) under ESD stress is investigated in this work. Single Fin (3-Sheet) ggNFET devices exhibit multiple instability points in the TLP-IV characteristic around the snapback region. Each of these instabilities was found to be arising due to non-uniform sheet turn-on and was independent of the presence of body contact. However, this instability was more severe, with a decreased body distance from the source. Furthermore, the sequence of turn-on was found to be dependent on the TLP current ramp rate. A 24-Fin (72 Sheet) ggNFET was simulated to reproduce the current filament like behavior. These 24- Fin simulations revealed a more severe low-current instability due to both non-uniform sheet turn-on and non-uniform Fin turn-on. For a smaller body to source contact distance, this non-uniform turn-on was seen to result in an early failure of the device.**

***Index Terms*—Electrostatic discharge, Vertically stacked Nanosheet, ggNMOS, Non-Uniform Sheet Turn-on, Technology Computer Aided Design (TCAD).**

I. INTRODUCTION

For technology scaling beyond FinFETs and Fully Depleted Silicon-On-Insulator, Gate-all-around (GAA) Nanowires and Nanosheets are acknowledged as likely candidates owing to their superior electrostatic control. The vertical stacking enables further scaling of the layout area. However, due to reduced silicon volume resulting in poor heat dissipation, these devices are vulnerable to ESD stress. Therefore, a detailed understanding of failure mechanisms and techniques to engineer their ESD protection elements' failure becomes critical. The previous attempts in the literature on understanding the behavior of ESD protection elements in Nanowires and Nanosheets have been limited to ESD diodes [1]-[3]. In this work, physical insights into turn-on and subsequent failure of grounded gate N-Vertically stacked nanosheet FET (ggNFET) is developed using detailed 3-D TCAD simulations. Furthermore, 24-Fin (72-sheet) ggNFET is simulated to reproduce the possible current filament behavior in them.

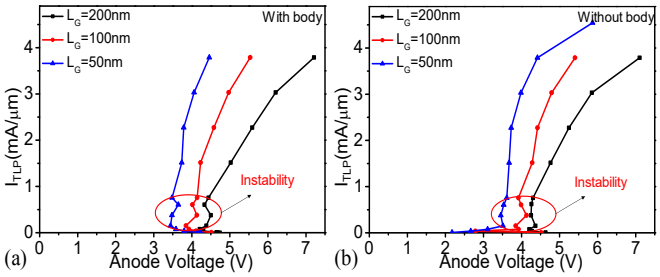

Fig. 2. TLP I-V Characteristics of GGNFET Nanosheet (a) with and (b) without body contact for varied gate lengths. There is a clear indicator of electrothermal instability at lower injected currents in these devices. Furthermore, despite removing the body contact the instability continues to exist. This indicates that the presence of this instability is independent of layout placement.

All the explorations in this work are done based on Sentaurus 3-D TCAD simulations. The TLP stressed current has a rise time of 10ns and a pulse width of 100ns. The quasi-static TLP-IV curve is extracted by averaging the voltage between 60ns to 90ns. Fig. 1c-d shows the TCAD calibration of appropriate mobility models and sheet confinement under DC operation for both a nanowire [4] and nanosheet [5] FET under DC operation. Thermal boundary conditions are taken into consideration to account for transient self-heating effects in the device under an ESD like event. Thermal resistances

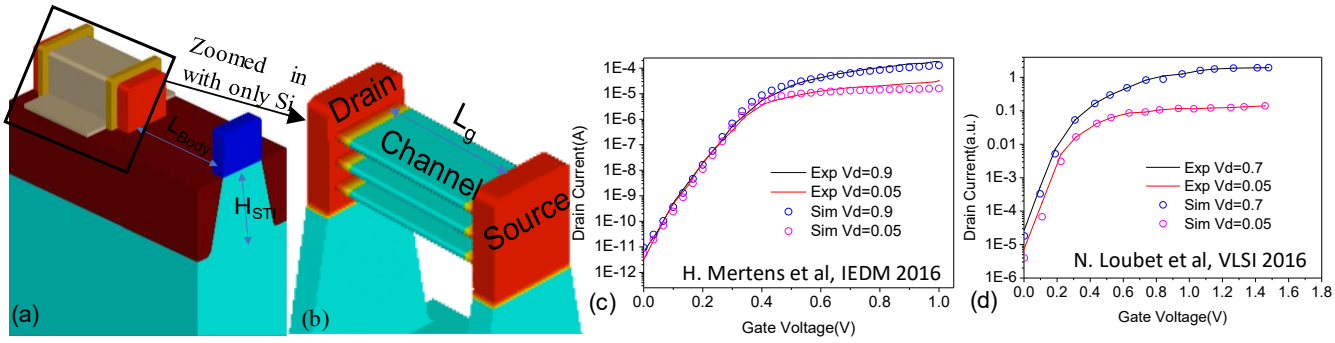

Fig. 1: (a)-(b) Isometric view of the nanosheet used for understanding their behavior under ESD stress. (c) & (d) TCAD calibration of mobility models and sheet confinement under DC operation in nanowire [4] and nanosheet [5] respectively.

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equivalent to back-end metal interconnect, and interlayer dielectric was considered.

II. Device under Test and Observations

Fig. 1a-b depicts the isometric view of the vertically stacked nanosheet FET under investigation in this work. Each fin has 3-Sheets and an isolated body contact at a distance Lbody from the source. The gate stack is wrapped over the sheets providing electrostatic control from all directions. Typically for ESD protection using ggN-FET, an array with a larger number (~500 Fins) of FETs is required. However, due to computational complexities, such a large array of the ggN-FET array can not be simulated on TCAD. This makes it challenging to capture the current filament dynamics in the device. An STI with a depth of 100nm is placed between the drain and source fin to exaggerate the filament characteristics. This helps capture the effect of filament in a simulation environment with 24 fin(/72 sheets), which is far lesser than the actual number of ggN-FETs present in an array for ESD protection.

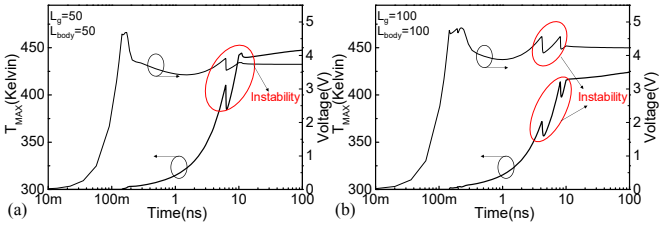


Fig. 3. Transient voltage and maximum lattice temperature for a ggNFET Nanosheet with gate and body length of (a) 50nm and (b) 100nm for injected TLP current @ 40% of It2. There are 2 instability points in the transient plot after the first bipolar turn-on. This instability is clearly more severe for lower body lengths (despite having lower gate lengths).

In this work, three sets of test cases have been studied:(1) Lg=200nm Lbody=100nm (2) Lg= 100nm Lbody= 100nm (3) Lg=50nm Lbody=50nm. In the third case, both body and gate length has been changed simultaneously to estimate the dominant engineering parameter among body and gate length. **Fig. 2a** depicts TLP-IV of the ggNFET device with the body contact in the three test cases described above. The holding voltage and dynamic on-resistance increase with gate length as expected. However, these devices show a peculiar low current instability right after the snapback region. Furthermore, TLP-IV of these devices extracted without body contact (**Fig. 2b**) also showed a similar instability, indicating that this instability is independent of the presence of body contact. In the next section, using transient extracted graphs and 3-D TCAD contours, an attempt is made to understand this instability.

III. Single Fin Instability

To further investigate this instability, transient maximum lattice temperature and transient voltage of the device in the test case (2) and (3) extracted at 40% of IT2 are shown in **Fig. 3a** and **Fig. 3b**, respectively. These plots reveal two

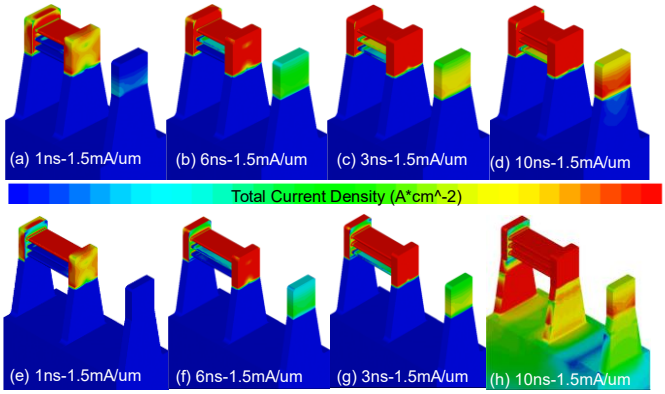


Fig. 4. Conduction current density of ggNFET Nanosheet with a gate length of (a)-(d) 50nm and (e)-(h) 100nm extracted at different times under ESD stress. Sheet turn-on doesn't happen uniformly resulting in multiple instability points in TLP-IV. The turn-on starts with either the top sheet or the bottom sheet and eventually all sheets turn-on at higher current(/time).

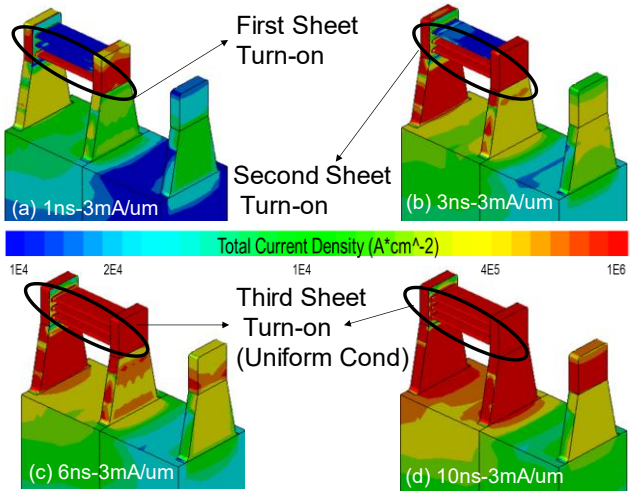


Fig. 5. (a)-(d) Conduction current density of ggNFET Nanosheet with Lg=100nm and injected current at 80% It2(i.e. double the rate at which TLP current is increased compared to Fig. 6 since the rise time is constant). At higher TLP current ramp rate the bottom most sheet turn-on first.

distinct instabilities after the first bipolar turn-on. Furthermore, the severity of these instabilities was found to increase with a decrease in source to body contact distance. **Fig. 4 a-d** and **Fig. 4e-h** depicts the conduction current density contour of GGNFET in the test cases (2) and (3) respectively for different times at an injected TLP current @40% of It2. The bipolar turn-on of these devices starts with the top (**Fig. 4a,e**) sheet and eventually spreads to the subsequent sheets below them at a higher injected current(/time). Comparing the devices with L_{body}=50 (**Fig. 4a-d**) and L_{body}=100 (**Fig. 4e-h**), in those devices with a lower-body to source contact distance, the turn-on of the respective sheets are slower. This results in increased severity of instability in those devices with lower body to source contact distance. **Fig. 4a-d** shows conduction current density of

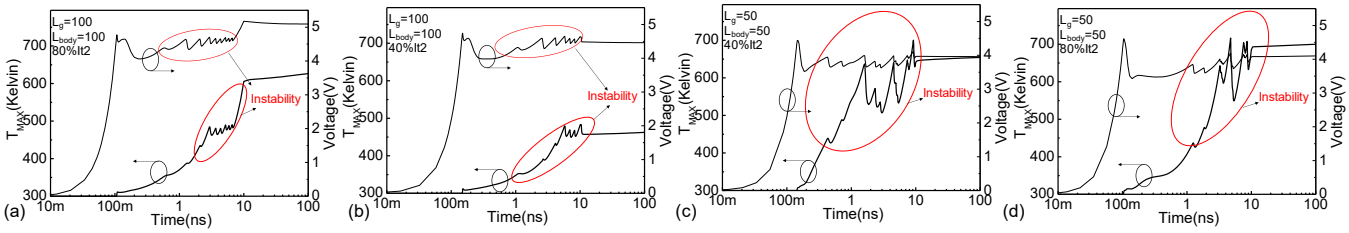


Fig. 6. Transient voltage and maximum lattice temperature for a 24-Fin Nanosheet ggNFET with gate length and body length of (a)-(b) 50nm and (c)-(d) 100nm for and injected current @40% & 80% of It2. Unlike single fin device (3 sheets) the 24-Fin (72 sheets) devices exhibit multiple instabilities in their transient behavior. In a 24-Fin configuration (@ 40% It2) the effect of decreased body length is more severe than in a single fin one which results in a 200-kelvin difference in the quasi-static maximum lattice temperature compared to a mere 20-kelvin difference in the latter.

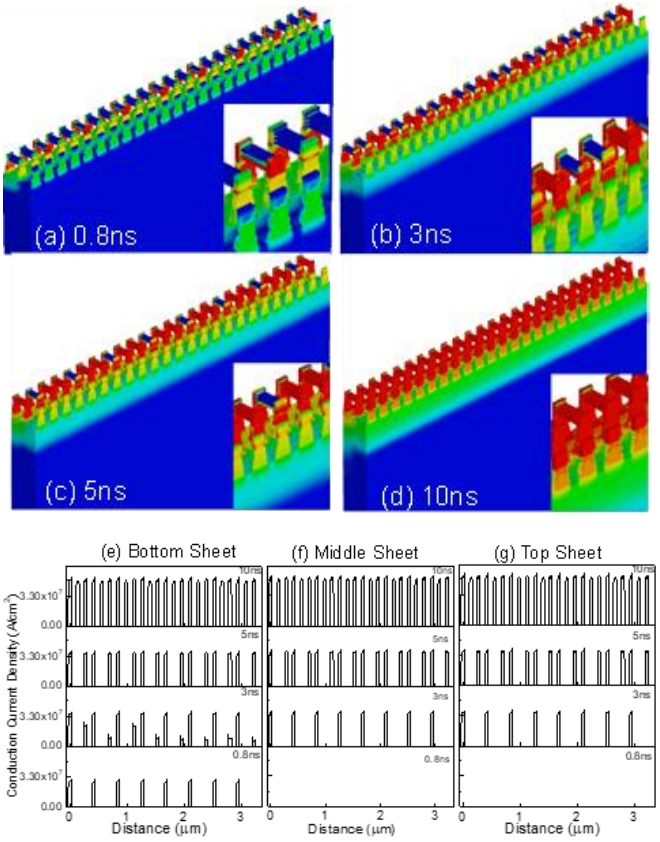


Fig. 7. Conduction current density of 24-Fin ggNFET Nanosheet (Lg, Lbody=100nm) plotted for different times and an injected TLP current @ 80% of It2. At (a) 0.8ns the bottom sheet of every third fin turns-on. At (b) 3ns all the three sheets of every third fin turn-on respectively. Furthermore @ (c) 5ns the turn-on of the sheets adjacent to the fins already turned on happens in the same sequence. And finally, @ (d) 10ns the turn-on of of the last fin (Third fin among the set of three fins) happens resulting in uniform turn-on. (e), (f) and (g) represents the extracted conduction current density at the midpoint of the bottom, middle and top sheet respectively for different times. From these graphs (**Fig. 7e-g**) the instability can be clearly seen at smaller times. This entire sequence of events is summarized in the flow chart shown above indicating conditions for both filament and non-filament driven failures.

ggNFET for test case 2 and an injected TLP current @ 80% of It2. In these device contours with a higher current ramp rate, the turn-on starts with the bottom-most sheet and eventually spreads to top sheets. In the next section, the manifestation of this instability in a larger array of this ggNFET will be studied to understand the current filament behavior.

IV. Multi-Fin Behavior

A 24-Fin (72-sheet) variant of ggNFET was simulated under ESD stress to investigate current filament dynamics. **Fig. 6a-d** depicts the transient voltage and maximum lattice temperature in a 24-Fin ggNFET. Unlike the single fin transient data, the 24-Fin devices seem to have more instabilities and depend on the injected current. Furthermore, the instability is more severely affecting the quasi-static maximum lattice temperature (**Fig. 6a, c**) at lower injected currents. Therefore, a 200K difference in maximum lattice temperature between devices 2 and 3 for injected current @ 40% It2 can be seen. From **Fig. 6a** and **Fig .6b**, the quasi-static lattice temperature in device 3 doesn't change significantly despite increasing the injected current by 2-fold. However, for device 3 the device reaches a stale transient voltage (/Temperature) within the current rise time.

To probe further into current filament dynamics of a 24-Fin ggNFET, the conduction current density is extracted in **Fig. 7a-d** for different times. Till the first bipolar trigger happens the conduction is limited between the reverse bias diode present across the drain and body contacts resulting in uniform current conduction across the devices. At t=0.8ns (**Fig. 7a, Fig.7e-g**), enough impact ionization generated carriers to trigger bipolar associated with a few sheets. Therefore, the bottom sheet of every third (For a 3-sheet per fin device) fin is turned-on. This causes a localized hot-spot and, thus, a sudden increase in maximum lattice temperature. Subsequently, at higher times (t= 3ns **Fig. 7b, Fig. 7e-g**), all sheets of every third fin are turned on. As the current (/time) increases, this process of current filament spreading happens in the fin next to the already turned fin (**Fig. 7c, Fig.7e-g**). Eventually, at higher injected currents (/time), all the fins turn-on (**Fig. d, Fig.7e-g**), relaxing the lattice temperature (**Fig. 6d**). From this analysis, it can be concluded that the turn-on in a multi-finger ggNFET with a sufficiently large number of fins happen in sets of 3-Fin at a time.

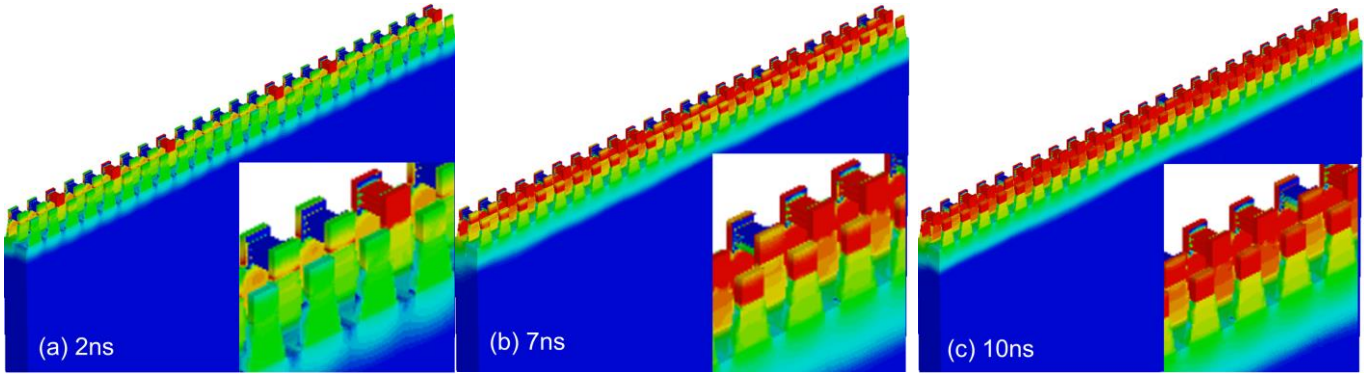
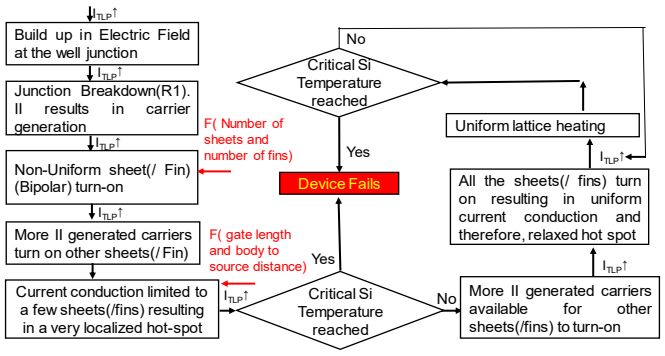


Fig. 8. Conduction current density of 24-Fin ggNFET Nanosheet (Lg, Lbody=50) plotted for different times and an injected TLP current @ 80% of It2. The severity of non-uniformity in turn on increases with decrease in body length. At body length=50nm and an injected current @ 80% It2(@ 7ns) none of the sheets of every third fin have turned-on comparison to device with body length=100nm with complete turn-on. Even at the end of the rise time(10ns) not all the sheets have turned-on. The sharp peak in the maximum lattice temperature seen in **Fig. 5(a)-(b)** can be attributed to this.



Flow Chart Summarizing the sequence of events leading to filament driven failure in Vertically Stacked Nanosheet Transistors

Fig. 8a-c depicts the conduction current density contour of device 3 extracted for and injected current @ 80% of It2. At lower currents (**Fig. 8a-b**), the device follows a similar turn-on mechanism described in the previous paragraph. However, **Fig. 8c** extracted @ the end of rise-time shows 2-sheets of every third fin still not turned on. Therefore, in these devices the failure threshold is strongly affected by the filament characteristics. Furthermore, for a larger array of fins, this non-uniform sheet (/Fins) can result in a filament driven early failure even at sufficiently large source to body contact lengths. Finally, this entire sequence of events is summarized in the flowchart, indicating conditions that determine final device failure threshold.

V. Conclusion

Using a well-calibrated 3-D TCAD setup, Vertically Stacked Nanosheet ggNFET was investigated under ESD stress. The TLP-IV and the transient voltage across the single fin device revealed two distinct instabilities after the first bipolar trigger. After further investigation, it was found the instability was due to non-uniform sheet turn-on. Furthermore, this instability was found to be independent of the presence of body contact and strongly dependent on the body to source contact distance. The conduction current density contour extracted for different injected TLP current suggested that the sheet turn-on sequence was dependent on the current ramp rate. To investigate current filament phenomena, a 24-Fin (72-Sheet) device was simulated. This revealed a more severe non-uniformity in turn-on among the various fins (/sheets), resulting in a higher number of instabilities in their transient voltage. Further investigation using current density contour revealed that for devices with the lower body to source distance, this non-uniform turn-on could result in early filament driven failure. The instability can be much more severe in devices with a larger array of fins, even for larger bodies to source length. Therefore, the future part of this work will be focused on understanding the effect of various engineering techniques to modify (/improve) the current filament behavior of this device.

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