Insights into the System-Level IEC ESD Failure in High Voltage DeNMOS-SCR for Automotive Applications

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Abstract - A unique failure mechanism for IEC stress through a common-mode choke is investigated. Minor variations in the stress current waveform shape for specific IEC stress levels are found to cause an unexpected window failure. 3D TCAD simulations are used to understand the device behavior and failure under the peculiar two-pulse shaped IEC current waveform. Device sensitivity to different components in the stimulus is studied in detail.

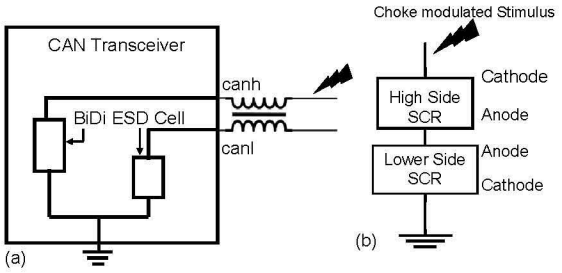
I. Introduction

Electrostatic Discharge (ESD) protection design is particularly challenging in automotive applications because product requirements often dictate qualification for a variety of stress models in addition to HBM and CDM. For example, the communication pins in automotive environments, like CAN and LIN, must be designed to protect against system-level stresses; e.g., IEC 61000-4-2. High voltage LDMOS/DeNMOS devices cannot be used at the high voltage pins as their failure current per unit area is small, resulting in unacceptably large cell size and capacitance [1]. The low failure current levels in high voltage LDMOS/DeNMOS devices are attributed to space charge modulation (SCM) induced filament formation at the onset voltage snapback [1]. High-holding voltage ESD solutions, such as PNPs and NPNs, also exhibit a relatively low failure current per unit area, making on-chip system-level protection a significant challenge because of the large ESD current requirements.

In contrast to high-holding voltage devices, snapback devices that operate in conductivity modulated mode can sustain very high ESD current per unit area [2]. Thus, one of the most area efficient solutions for on-chip system-level ESD protection is the high-voltage Silicon Controlled Rectifier (SCR) device in an LDMOS/DeMOS process [3]. However, there are multiple challenges in using the HV-SCR as a protection device. For example, the problem of power scalability of such devices for long duration discharges was highlighted in [4-5]. Additionally, HV-SCRs are found to be vulnerable for IEC system-level failures when stressed with a common-mode choke in the path [6]. The alteration of the current waveform shape with a common-mode choke in the stress path can be attributed to high-current saturation of the choke [4]. The high current saturation of choke was also demonstrated in [7] with Transmission Line Pulse (TLP) stressing the choke alone. Previous works [6] have overlooked the change in shape of the waveform with choke and tried to address the problem simply as an increased rise-time effect. In this work, we study the behavior of the HV-SCR when stressed by the unusual stimulus caused by choke saturation.

II. Choke Saturation Problems Under High Current ESD Stress

The CAN pins in the automotive ICs presented in this work are protected using a high-voltage bidirectional DeNMOS-based SCR device at both CAN high and low pins. Two MOS-SCR devices are connected in a back-to-back configuration, as depicted in Fig.1. During positive/negative IEC strike, the top MOS-SCR will be in diode/SCR mode and the bottom MOS-SCR is in SCR/diode mode. The common-mode (CM) choke is added to



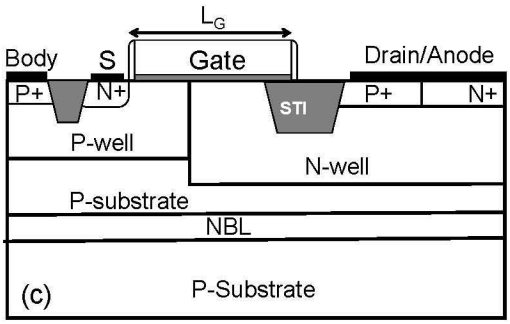


Figure 1: (a) Schematic representation of choke connection to the DUT. (b) Representation of how a single ended SCR is connected in a bidirectional configuration to withstand both positive and negative ESD discharges. (c) The Cross-sectional view of a DeNMOS SCR.

Table-1: IEC results summarizing the pass/fail information at every stress level for both with and without choke cases. Device is found to fail for -3kV stress level with choke, however, passes all lower and higher stress levels. Whereas the same behavior is not observed when choke is not present in the stress path. The device survives every stress level.

IEC Stress Level	With choke Pass/Fail	Without choke Pass/Fail
-1 KV	Pass	Pass
-2KV	Pass	Pass
-3KV	Fail	Pass
-4KV	Pass	Pass
(greater than -5 kV)	Pass	Pass

the CAN pins to reject the common-mode noise at the differential communication pins, as depicted in Fig. 1(a). The common-mode choke is a transformer that presents an inductive load to the CAN pins. When the communication pins are tested for system-level ESD protection, they are required to qualify for two scenarios: Direct stress, in which the ESD gun touches one of the CAN pins, and an indirect test, in which CAN pins are stressed through a CM choke. However, CM chokes are not designed to handle the large currents that a system level ESD event produces [7]. The core saturation effect at high currents in CM inductive chokes has previously been found to cause unexpectedly low system-level ESD failure levels [6-7].

Table 1 presents the IEC test results for the direct and indirect tests. For the direct test, the automotive IC was qualified for all stress levels. However, with a CM choke in the ESD stress path, the IC passed low and high stress levels, but failed at -3kV. When the same experiment was repeated with much smaller step sizes (200 V) between -3 kV and -4 kV, failures were observed in a very fine window of stress levels.

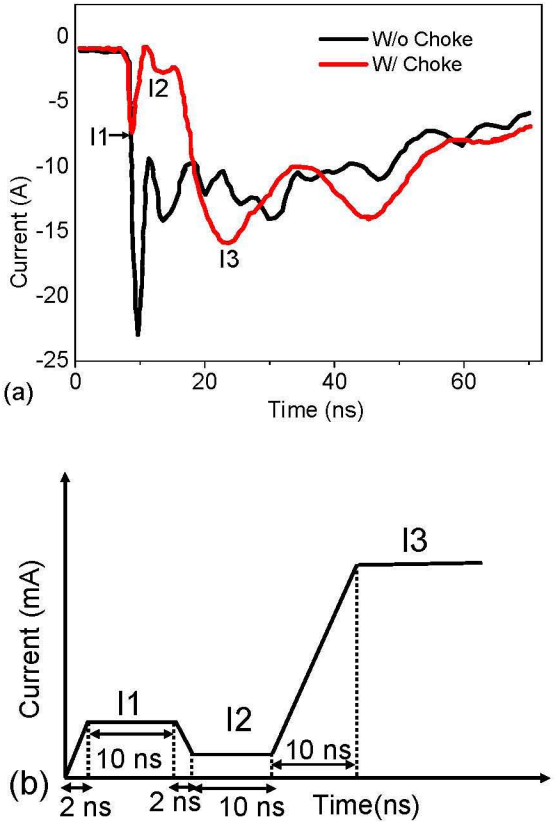


Figure 2: Measured IEC current waveforms (at the gun tip) for a -5 KV pre-charge level for both direct contact stress and stress through the choke. The first current peak I1 is present for the stress through choke followed by a high amplitude second pulse. The residual current between both pulses (I2) changes with pre-charge voltage, setup etc. However, the direct contact discharge waveform has one sharp current peak typically seen in most IEC measurements. (b) The idealized two peak current waveform for 3D TCAD studies.

The IEC current waveform measured at the gun tip for the case of stress through choke exhibits a two-pulse current waveform, depicted in Fig. 2(a). Unlike the traditional IEC 61000-4-2 contact discharge current waveform, there exists a first peak with small current (I1), followed by reduction in peak to a residual current (I2) for a certain time duration, followed by a larger amplitude second current peak (I3). It is worth highlighting here that the magnitude of I1 and I2 vary depending on the pre-charge stress level and various system conditions. This variation of first peak current (I1) and residual current magnitude (I2) is the source of window failures, as it in turn impacts the SCR turn on behavior. 3D TCAD simulations are used to understand the device behavior under such a peculiar stimulus. The idealized current waveform used for 3D TCAD investigations is shown in Fig. 2(b).

III. Understanding the Root Cause of Failure

An ideal current source is used as the stress stimulus during electrothermal TCAD simulations with proper electrical and thermal contacts. Cathode and gate are shorted (to study without MOS-current) with a negative current pulse applied at the cathode.

A. Understanding from TLP Characteristics

Although TLP itself cannot capture the observed "window" failures, it is worth analyzing the simulated TLP characteristics. Fig. 3 depicts the 100 ns TLP I-V characteristics extracted from 3D TCAD simulations. The Fig. 3 (b) shows the extracted maximum temperature for each stress (current in this case) value. It can be observed that the lattice temperature is highest at stimulus current levels near the SCR's holding current and then decreases significantly as stimulus current increases. This was previously observed to cause failure near snapback for long duration pulse discharges (PW>100ns) measured with a high-impedance load line TLP system [5]. The observation that non-uniform conduction near the holding point (at lower current level) leads to increased lattice heating is instructive for understanding the failure observed during IEC stress through a common-mode choke.

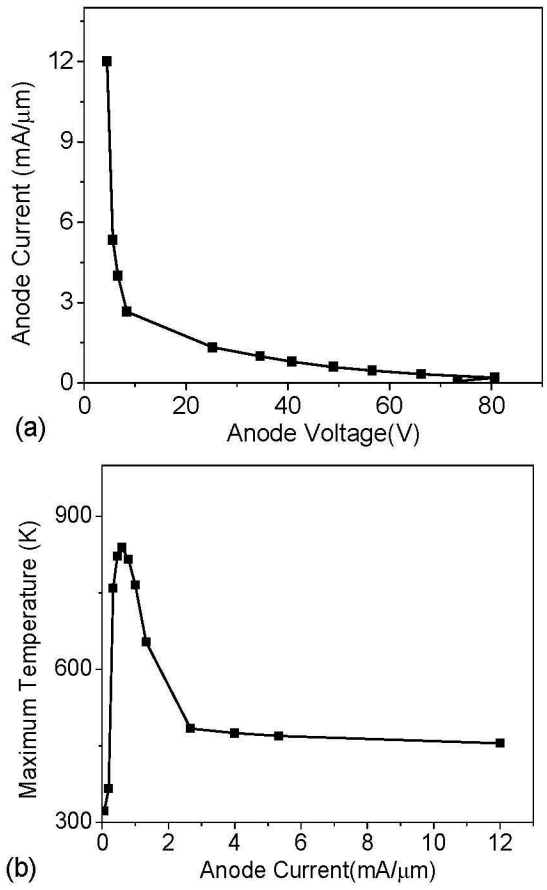


Figure 3: 3D TCAD simulated (a) TLP I-V characteristics of DeNMOS-SCR stressed with 100 ns duration pulses (b) Maximum Lattice temperature plotted as function of stress current. Device is observed to heat up (higher lattice temp.) at lower current values, whereas lower temperature is observed at higher current values.

B. Root Cause for Failure Under Choke/Two Pulse Stimulus

The DeNMOS-SCR was simulated using 3D TCAD and stressed with the pulse shown in Fig. 2 (b) that is an idealized version of the current waveform measured for an IEC 61000-4-2 discharge through the CM choke. Fig. 4 shows device voltage response and maximum lattice temperature inside the DeNMOS SCR during the stimulus. While I1 is applied, voltage snapback occurs as the SCR turns on. It is also evident that snapback in I1 is not deep (region-I in Fig. 4). The current density in I1 indicates that the SCR cannot turn on uniformly (Fig. 5) and lattice heating in I1

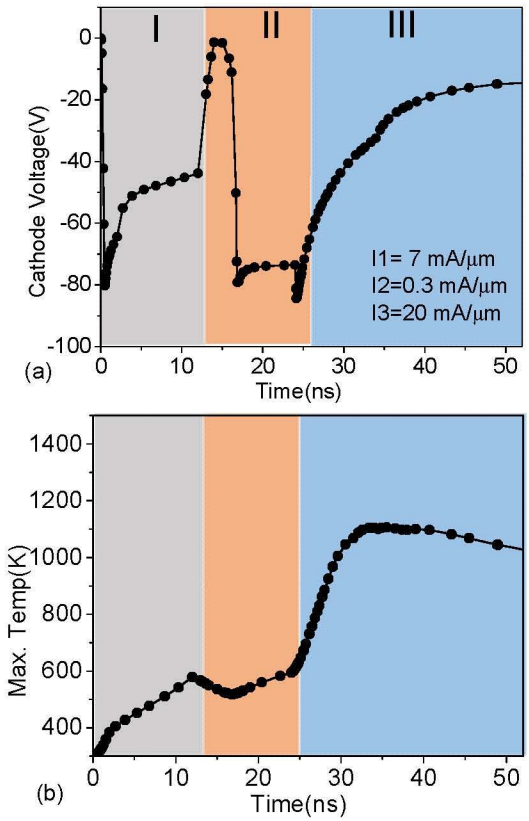


Figure 4: 3D TCAD extracted device response for the two-pulse stimulus. (a) Transient cathode voltage (b) maximum lattice temperature as a function of stress time. SCR triggering causes voltage snapback in region I (during first pulse). Ramp down of current in region-II, reduces the voltage further. However, after some time in II, voltage further shoot-up until ramp up of current in region-III. Peak temperature observed during ramp of I3 is critical in deciding the device failure in this kind of stimulus.

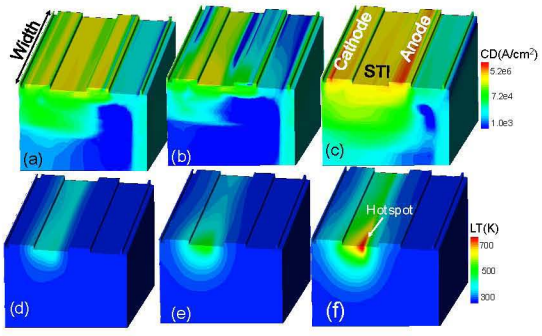


Figure 5: Conduction current density (a,b,c) and lattice temperature(d,e,f) extracted at end of I1 (a and d), end of I2 (b and e) and during ramp up of I3 (c and d). Smaller current in I1 causes non-uniform SCR turn-on. During I2, this causes non uniform turn-off of SCR and stronger current crowding which becomes significant during ramp up of larger IEC current pulse I3. The stimulus currents are same as in fig. 4.

is also non-uniform (Fig. 5). As the stimulus transitions to the I2 region, ramp down of current causes reduction (absolute number) in cathode voltage (Fig. 4), until the carrier concentration in the N-well and P-well decrease significantly and the SCR cannot maintain the low-impedance state, after which a significant increase in cathode voltage is observed. This is where a low current filament is formed (Fig. 5). As the current begins to increase during the rising edge of I3, this filament intensifies and an increase in current density inside the filament causes a localized hotspot to form, resulting in a peak in the lattice temperature.

It is this peak during I3 that causes device failure under two pulse stimuli when a choke is present in the IEC discharge path. It is observed that the device will not see such a high lattice temperature peak during ramp-up of I3 (for the same current value in I3) when I1 and I2 current pulses are not present. Hence, this failure is particular to the shape of the stimulus that the SCR experiences under choke saturation.

IV. Failure Sensitivity for Different Stimulus Components

In this section we investigate the effect of different current components (I1, I2) of the unique pulse shape and their influence on the device failure. For all these studies, I3 is kept constant at 20 mA/μm.

A. Sensitivity of Device Failure for First Pulse Magnitude (I1)

The sensitivity of device failure (peak temperature during ramp up of I3) is studied against the magnitude of current that is injected into SCR during I1. Several observations can be made from Fig. 6, which shows cathode voltage and maximum lattice temperature plotted for different current values in I1 (I2 andI3 are kept unchanged for these studies):

- The increase in current in I1 causes deeper voltage snapback during the I1 pulse
- As I1 increases, the SCR takes a longer time to turn off, accompanied by a "snap up" in its cathode voltage.
- Maximum lattice temperature during I3 first increases and then decreases to lower values with increase in injected current in I1

The deeper snapback at higher I1 values is attributed to stronger and more uniform SCR turn-on, as shown in Fig. 7. Larger current density in I1 implies that carriers take a longer time to recombine when current at the cathode is ramped down to I2. This also found to cause more uniform current distribution during I2 Fig. 7), which

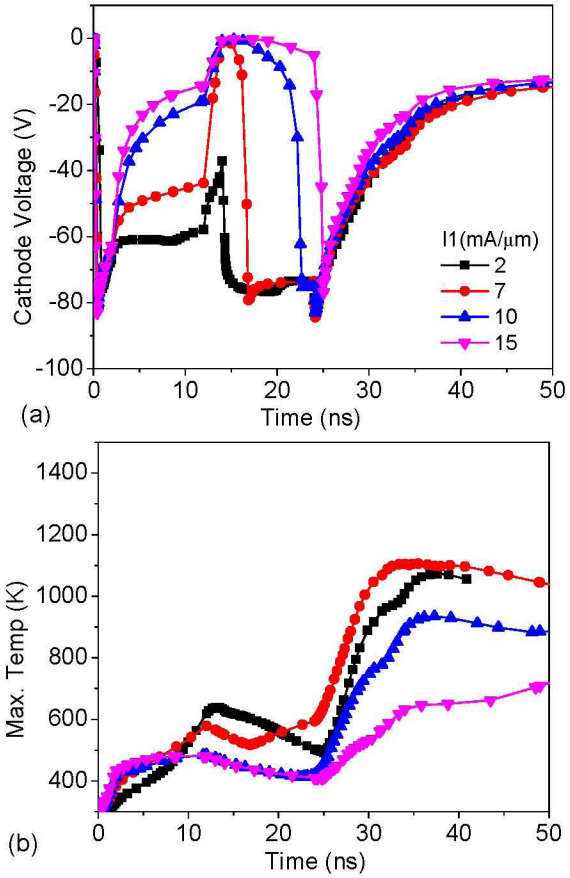


Figure 6: 3D TCAD extracted (a) cathode voltage and (b) maximum lattice temperature inside the device plotted as function of time for different current values in the first pulse (I1). In these studies, I2 (0.3 mA/μm) and I3 (20 mA/μm) are kept constant. The peak temperature in during I3 found to have a maximum value in a window of currents in I1, beyond which it decreases drastically.

mitigates filament formation during ramp-up of I3. Even if there is some non-uniform conduction during I3, the distribution of carriers across the device in I2 causes faster filament spreading and lower lattice temperature.

B. Sensitivity of Device Failure for Second Pulse Magnitude (I2)

The risk of choke-induced failures is also sensitive to the residual current magnitude (I2) that is

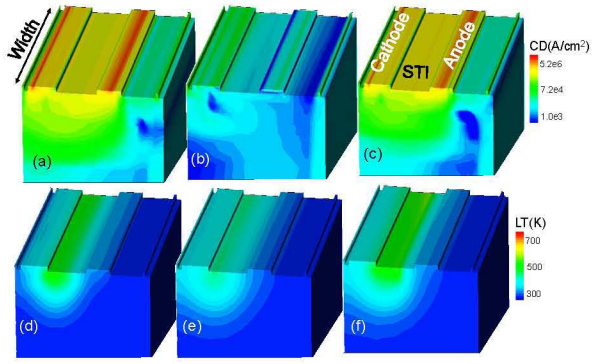


Figure 7: Conduction current density (a,b,c) and lattice temperature(d,e,f) extracted at end of I1 (a and d), end of I2 (b and e) and during the ramp up of I3 (c andd). Injecting larger current through SCR in I1(15 mA/um in this case), causes more uniform SCR turn on in I1, which eventually causes more uniform turn-off in I2 and eliminates the filament induced SCR failure in larger IEC current pulse I3.

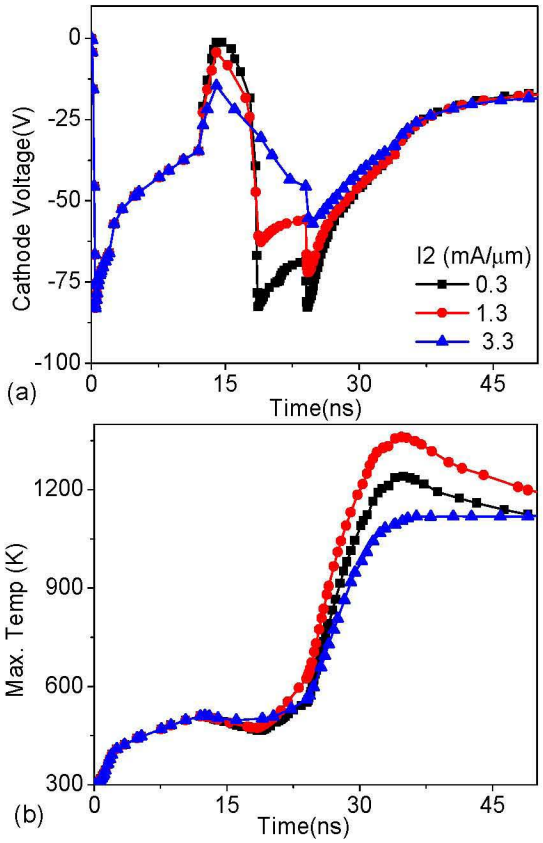


Figure 8: (a) cathode voltage and (b) maximum lattice temperature plotted as a function stress time for different current levels in I2 region of the stimulus. The I1 for this experiment is chosen to be 7 mA/μm. The peak temperature first increases with I2 and then decreases with further increases once I2 exceeds 1.3 mA/μm.

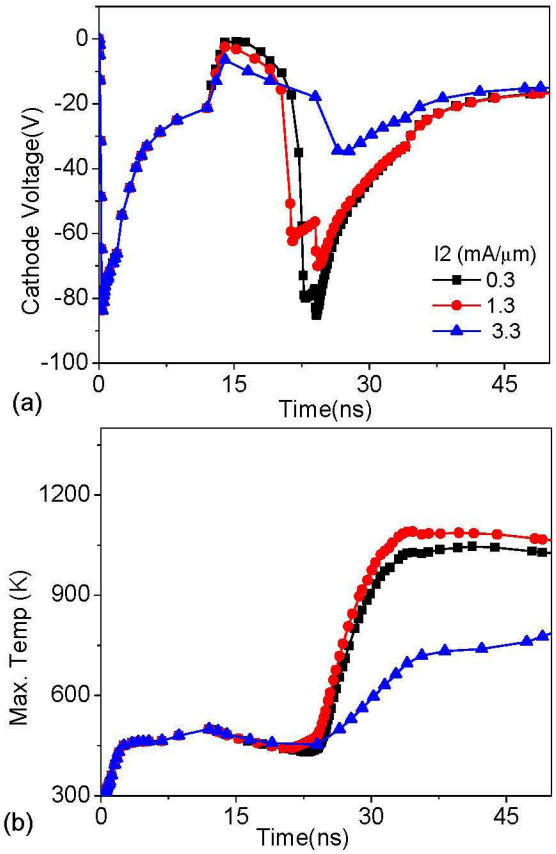


Figure 9: (a) cathode voltage and (b) maximum lattice temperature plotted as a function stress time for different current levels in I2. The I1 for this experiment is 10 mA/μm. The larger current in I1 reduces the temperature swing or sensitivity for changes in I2.

between the two current peaks (I1 and I3). When I1 is assumed to be a lower value (around 7 mA/μm in this case), sensitivity to I2 is amplified, as shown in Fig. 8. Further, there is a window observed in I2 for which the peak temperature in I2 is a maximum. At lower I2 values, current density inside the filament is reduced and the peak does not occur during I2, resulting in uniform turn-on in the I3 region. Further, the swing in peak temperature as a function of I2 depends on the magnitude of I1. At higher I1, the device conducts more uniformly and turns off more uniformly in I2. In this case, the magnitude of I2 does not strongly affect the peak value, as the filament is not strong in I2. Additionally, a dramatic reduction in peak temperature observed at higher values of I2 when I1 is larger. This is further attributed to a strongly turned on SCR in I1; in this case, the SCR will not substantially turn off in I2 and will continue to conduct in SCR mode as the I3 pulse arrives.

C. Two Pulse Stimulus Behavior for Different SCR Strength

The behavior of two MOS-SCR designs with different SCR strength was studied to understand the two-pulse device behavior Fig. 10 presents a comparison of simulated voltage and peak

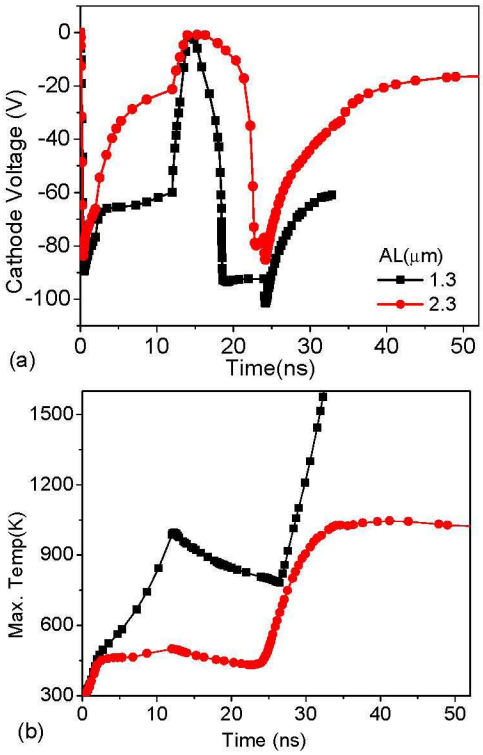


Figure 10: (a) cathode voltage and (b) maximum lattice temperature as a function stress time for different SCR designs when they are stressed with same stimulus (two pulse stimuli). The deeper snapback in I1 and small temperature peak in I3 is observed for device with strong SCR (larger P+ anode length AL) action compared to the weaker SCR device (smaller AL).

temperature for two SCRs during the two-pulse TCAD simulation. SCR strength in the designs is tweaked by changing the P+ anode length (emitter area for the inherent P-N-P). The stronger SCR device has a deeper snapback in I1 region when stressed with same stimulus current. The deeper snapback is attributed to strong SCR action and more uniform current conduction in I1 (smaller temperature is also observed in I1 region). The stronger SCR design also takes a longer time to transition into the filament mode during I2 (where cathode voltage reaches to higher value). This implies that the stronger SCR design conducts more uniformly in the I3 region and reduces the peak temperature during I3. Hence, efforts to

mitigate the SCR IEC-through-choke sensitivity should be focused on increasing the strength of SCR action based on the results presented in Fig. 10.

V. Conclusion

A choke-induced ESD failure in a system-level automotive ESD environment is revisited. Change in current pulse waveform shape that occurs within a narrow range of IEC stress levels is found to be the concern. A weak current pulse (first pulse) prior to the large IEC current peak (second pulse) was observed to cause filamentation inside the device, which eventually causes device failure during the larger second pulse. Higher first pulse current can mitigate the device failure during large second current pulse; this is attributed to uniform turn-on of the SCR during first pulse, which in turn causes a weak filament inside the device and uniform conduction during the larger IEC second pulse. The residual current between first and second pulse is also found to significantly impact the failure. Higher residual current results in more uniform turn-off of the SCR going from first pulse to larger IEC current pulse, mitigating the filament formation during the larger second pulse. Finally, design with stronger SCR action is found to cause improved thermal distribution inside the device with the same two-pulse stimuli compared to a weaker SCR design.

VI. Acknowledgements

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